

ICECS 2007

**14th IEEE
International Conference
on Electronics, Circuits
and Systems**

Advance Program

December 11-14, 2007

Marrakech, Morocco



ICECS ²⁰⁰⁷

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Manifestation réalisée avec le concours du Ministère de l'Éducation Nationale, de l'Enseignement Supérieur de la Formation des Cadres et de la Recherche Scientifique et du CNRST

Welcome to ICECS 2007

On behalf of the IEEE-ICECS'2007 Organizing Committee and Technical Program Committee, we would like to welcome you for the first time to Morocco, and the beautiful city of Marrakech, during the week of 11-14 December 2007. ICECS'2007 is co-organized by l'Ecole Mohammadia d'Ingénieurs and l'Université de Montréal.

The wide range of topics covered by ICECS drew over 500 submissions from 51 countries. These were assigned by the track chairs to over 354 reviewers, who performed the enormous task of reviewing them in a short time. We feel very much indebted to them for their invaluable help in keeping the level of ICECS to the high standard that our scientific community has grown to expect. Based on those reviews, 359 contributions were selected for presentation in a total of 67 regular or special lecture and poster sessions.

In addition, 6 Keynote speeches will be given by experts from Academia and industry: Andreas G. Andreou (Johns Hopkins U., USA), Giovanni De Micheli (EPF Lausanne, Switzerland), Mohammad S. Obaidat (Monmouth U., USA), Magdy A. Bayoumi (U. of Louisiana at Lafayette, USA), Didier Lattard (CEA, France), and Kiyoo Itoh (Hitachi, Japan). ICECS'2007 will also encompass six half day tutorials and an embedded tutorial given by renowned experts. A panel on globalization is also organized and this will surely offer an interesting exchange of ideas.

The IEEE ICECS conferences have evolved to be the most important annual Electronics, Circuits and Systems meeting in IEEE Region 8. This conference has the unique characteristic of building an intellectual bridge between the south and north coasts of the Mediterranean Sea. It has alternated between the two coasts since it was first held in Cairo, Egypt, one of the oldest cradles of Mediterranean civilisation. This year it will be held in Marrakech, an imperial city of Morocco, which was, like this conference, a meeting point between the civilizations of the North and the South.

We would like to take this opportunity to thank all the members of the Steering and International Advisory Committees, the Organizing Committee, the Technical Program Committee, the Special Sessions organisers, the Keynote Speakers, the Tutorial speakers, the Track Chairs and the many reviewers and most of all the authors for contributing their original work and presenting it at the conference. We would also like to thank the numerous volunteers that helped with the organisation. We extend our thanks to the different sponsors for their valuable help and generosity.

We are very proud to be hosting the ICECS conference for the first time in Morocco and we are pleased to have you in the beautiful and historical city of Marrakech. We hope you will enjoy the conference.



Driss Bouami



El Mostapha Aboulhamid



Mohsine Eleuldj



Mark Zwolinski

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Welcome reception

Date: Tuesday 10

Time: 17:30-19:30

Location: Royal Mirage Ricardo Restaurant

Banquet

Date: Thursday December 13

Time: 19:30-23:30

Location: Chez Ali, Safi Road, 12 km, Phone: 024 30 77 30, Fax: 024 30 93 82

Departure at 19:30 by bus

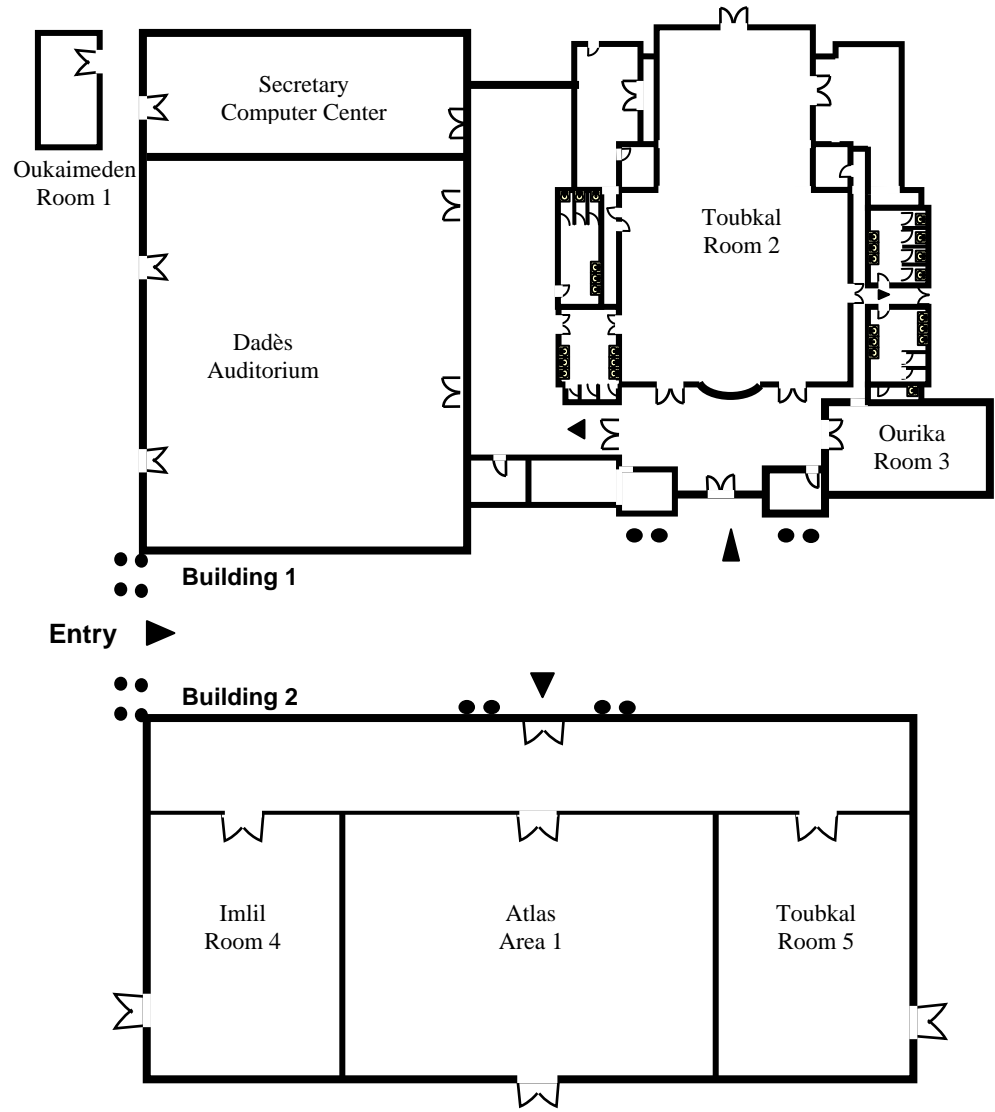
Return to Royal Mirage: 23:30 by bus

Closing Ceremony

Location: Auditorium

Best paper awards and best student paper award will be presented during this ceremony

Conference Center



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ICECS 2007 Program

Tuesday, December 11, 2007

8:00	19:30	Registration
8:30	11:30	Tutorials
T1 , Room 2		<i>State-of-the-art continuous-time filters from scratch</i> Un-Ku Moon, Oregon State U., USA
T2 , Room 4		<i>Magnetotactic bacteria as controlled components in microelectronic circuits</i> Sylvain Martel, Polytechnique, Montreal, Canada
T3 , Room 5		<i>Managing Power Consumption and Variability in Nanometer Circuits</i> Mohab H. Anis, Waterloo U., Canada
14:30	17:30	Tutorials
T4 , Room 2		<i>Analog and asynchronous variation-aware circuits</i> Alyssa B. Apsel (Cornell U., USA), Rajit Manohar (Cornell U., USA), Alain J. Martin (Caltech, USA)
T5 , Room 4		<i>Dependability issues in SRAM-based FPGA design</i> Régis Leveugle, TIMA Grenoble, France
T6 , Room 5		<i>Circuit Techniques for Operational Amplifier Speed and Accuracy Improvement: Analog Circuit Design with Structural Methodology</i> Vadim V. Ivanov (T.I.), I. M. Filanovsky (U. of Alberta, Canada)
17:30	19:30	Welcoming Reception

ICECS 2007 Program

Wednesday, December 12, 2007

8:00	19:00	Registration
		8:30-8:45 Opening
8:30	10:15	8:45-9:30 Keynote I : <i>Microsystems engineering from nano to micro and macro</i> Andreas G. Andreou, Johns Hopkins U., USA
		9:30-10:15 Keynote II : <i>New Design Paradigms: New Architectures for New technologies</i> Giovanni De Micheli, EPF Lausanne, Switzerland
10:15	10:40	Break Poster Session A (A3P)
10:40	12:10	Lecture Sessions 1.1 (A4L)
12:10	13:40	Lunch
13:40	14:25	Keynote III : <i>Wireless Sensors Networks: The Art of Integration</i> Magdy Bayoumi, U. of Louisiana at Lafayette, USA
14:30	16:00	Lecture Sessions 1.2 (A6L)
16:00	16:25	Break Poster Session B (A7P)
16:25	17:55	Lecture Sessions 1.3 (A8L)
18:00	19:00	Panel Discussion: <i>Globalization in the domain of circuits and Systems: Impacts, costs and benefits</i> Chair: Pierre Paulin, STMicroelectronics, Canada

ICECS 2007 Program

Thursday, December 13, 2007

8:00	19:00	Registration	
8:30	9:15	Keynote IV : <i>Trends and Challenges in Wireless Systems</i> Mohammad S. Obaidat, Monmouth U., USA	
9:20	10:50	Lecture Sessions 2.1 (B2L)	Embedded Tutorial (T7)
10:50	11:15	Break	Poster Session C (B3P)
11:15	12:45	Lecture Sessions 2.2 (B4L)	
12:45	14:00	Lunch	
14:00	15:30	Keynote V : <i>Trends in complex SoC Design: From technology variability to multiprocessor architectures</i> Didier Lattard, CEA, France	
		Keynote VI : <i>Low-Voltage Limitations and Challenges of Memory-Rich Nano-Scale CMOS LSIs</i> , Kiyoo Itoh, Hitachi, Japan	
15:35	17:05	Lecture Sessions 2.3 (B7L)	
17:05	17:30	Break	Poster Session D (B8P)
17:30	19:00	Lecture Sessions 2.4 (B9L)	
19:30	23:30	Banquet	

ICECS 2007 Program

Friday, December 14 2007

8:00	16:00	Registration
8:30	9:15	Invited Talk <i>SPRAM (SPin-transfer torque RAM) Design and its Impact on Digital Systems</i> Takayuki Kawahara, Hitachi, Japan
9:20	10:50	Lecture Sessions 3.1 (C2L)
10:50	11:15	Break Poster Session E (C3P)
11:15	12:45	Lecture Sessions 3.2 (C4L)
12:45	14:00	Lunch
14:00	15:30	Lecture Sessions 3.3 (C5L)
15:30	16:00	Closing Ceremony

Microsystems engineering from nano to micro and macro

Andreas G. Andreou, Johns Hopkins U., USA

Circuits and Systems Society's Distinguished Lecturer



Andreas G. Andreou received his Ph.D. in electrical engineering and computer science in 1986 from Johns Hopkins University. Between 1986 and 1989 he held post-doctoral fellow and associate research scientist positions in the Electrical and Computer engineering department while also a member of the professional staff at the Johns Hopkins Applied Physics Laboratory. Andreou became an assistant professor of Electrical and Computer engineering in 1989, associate professor in 1993 and professor in 1996. He is also a professor of Computer Science and of the Whitaker Biomedical Engineering Institute and director of the Institute's Fabrication and Lithography Facility in Clark Hall. He is the co-founder of the Johns Hopkins University Center for Language and Speech Processing. Between 2001 and 2003 he was the founding director of the ABET accredited undergraduate Computer Engineering program. In 1996 and 1997 he was a visiting professor of the computation and neural systems program at the California Institute of Technology. In 1989 and 1991 he was awarded the R.W. Hart Prize for his work on mixed analog/digital integrated circuits for space applications. He is the recipient of the 1995 and 1997 Myril B. Reed Best Paper Award and the 2000 IEEE Circuits and Systems Society, Darlington Best Paper Award. During the summer of 2001 he was a visiting professor in the department of systems engineering and machine intelligence at Tohoku University. In 2006, Prof. Andreou was elected as an IEEE Fellow and a distinguished lecturer of the IEEE EDS society. Andreou's research interests include sensors, micropower electronics, heterogeneous microsystems, and information processing in biological systems. He is a co-editor of the IEEE Press book: Low-Voltage/Low-Power Integrated Circuits and Systems, 1998 (translated in Japanese) and the Kluwer Academic Publishers book: Adaptive Resonance Theory Microchips, 1998. He is an associate editor of IEEE Transactions on Biomedical Circuits and Systems.

New Design Paradigms: New Architectures for New technologies

Giovanni De Micheli, EPF Lausanne, Switzerland



Giovanni De Micheli is Professor and Director of the Integrated Systems Centre at EPF Lausanne, Switzerland, and President of the Scientific Committee of CSEM, Neuchatel, Switzerland. Previously, he was Professor of Electrical Engineering at Stanford University. He holds a Nuclear Engineer degree (Politecnico di Milano, 1979), a M.S. and a Ph.D. degree in Electrical Engineering and Computer Science (University of California at Berkeley, 1980 and 1983).

His research interests include several aspects of design technologies for integrated circuits and systems, such as synthesis, hw/sw codesign and low-power design, as well as systems on heterogeneous platforms including electrical, optical, micromechanical and biological components. He is author of: *Synthesis and Optimization of Digital Circuits*, McGraw-Hill, 1994, co-author and/or co-editor of six other books and of over 300 technical articles. He is, or has been, member of the technical advisory board of several companies, including Magma Design Automation, Certess, Coware and STMicroelectronics.

Prof. De Micheli is the recipient of the 2003 IEEE Emanuel Piore Award for contributions to computer-aided synthesis of digital systems. He is a Fellow of ACM and IEEE. He received the Golden Jubilee Medal for outstanding contributions to the IEEE CAS Society in 2000. He received the 1987 D. Pederson Award for the best paper on the IEEE Transactions on CAD/ICAS, two Best Paper Awards at the Design Automation Conference, in 1983 and in 1993, and a Best Paper Award at the DATE Conference in 2005.

He has been serving IEEE in several capacities, namely: Division 1 Director (2008-9), co-founder and President Elect of the IEEE Council on EDA (2005-7), President of the IEEE CAS Society (2003), Editor in Chief of the IEEE Transactions on CAD/ICAS (1987-2001). He was Program Chair of the pHealth and VLSI SOC conferences in 2006. He was the Program and General Chair of the Design Automation Conference (DAC) in 1996-1997 and 2000 respectively. He was the Program and General Chair of the International Conference on Computer Design (ICCD) in 1988 and 1989 respectively. He is a founding member of the ALaRI institute at Universita' della Svizzera Italiana (USI), in Lugano, Switzerland, where he is currently scientific counselor.

New Wireless Sensors Networks: The Art of Integration

Magdy Bayoumi, U. of Louisiana, USA



Magdy A. Bayoumi is Director of The Center for Advanced Computer Studies (CACCS), and Department Head of the Computer Science Department at the University of Louisiana at Lafayette (UL Lafayette). He is also Edmiston Professor of Computer Engineering, and Lamson Professor of Computer Science. Dr. Bayoumi has been a faculty member in CACCS since 1985. He received B.Sc. and M.Sc. degrees in Electrical Engineering from Cairo University, Egypt; M.Sc. degree in Computer Engineering from Washington University, St. Louis; and Ph.D. degree in Electrical Engineering from the University of Windsor, Canada. Dr. Bayoumi is the recipient of the IEEE Circuits and Systems Society 2003 Education Award, and he is an IEEE Fellow. He was on the governor's commission for developing a comprehensive energy policy for the State of Louisiana. He represented the CAS Society on the IEEE National Committee on Engineering R&D policy, IEEE National Committee on Communication and Information Policy, and IEEE National Committee on Energy Policy. He was and has been Guest Editor (or Co-Guest Editor) of eight special issues in VLSI Signal Processing, Learning on Silicon, Multimedia Architecture, Digital and Computational Video, Perception on a Chip, and Systems on a Chip. He has given numerous invited lectures and talks nationally and internationally, and has consulted in industry. Dr. Bayoumi is the Vice President for Conferences of the IEEE (CAS) Society. He was Chair and Founder of "Circuits and Systems for Communication" Technical Committee. He was Chair of VLSI Systems and Applications (VSA) Technical Committee (TC). He was Associate or Regional Editor for different journals. Dr. Bayoumi served on the technology panel and advisory board of the U.S. Department of Education project, "Special Education Beyond Year 2010," 1990-1993. He was Vice President of Acadiana Technology Council. He was on the organizing committee for Acadiana's 3rd Internet Workshop, 1999. He gave the keynote speech in "Acadiana Y2K Workshop," 1999, Lafayette. He is a member of Lafayette Chamber of Commerce where he was a member of the Economic Development, Education, and Tourism Committees. Dr. Bayoumi was a technology columnist and writer of the Lafayette newspaper, "The Daily Advertiser".

Trends and Challenges in Wireless Systems

Mohammad S. Obaidat, Monmouth U., USA



Professor Mohammad S. Obaidat is an internationally well known academic/researcher/ scientist. He received his Ph.D. and M. S. degrees in Computer Engineering with a minor in Computer Science from The Ohio State University, Columbus, Ohio, USA. Dr. Obaidat is currently a tenured full Professor of Computer Science at Monmouth University, NJ, USA. Among his previous positions are Chair of the Department of Computer Science and Director of the Graduate Program at Monmouth University and a faculty member at the City University of New York.

He has published over three hundred and forty (340) refereed technical articles. He is the author of several books including the Best Selling Book, *Wireless Networks* (Wiley 2003), *Multiwavelength Optical LANs* (Wiley 2003), *APPLIED SYSTEM SIMULATION: Methodologies and Applications* (Kluwer/Springer 2003), *Security of e-Systems and Computer Networks* (Cambridge University Press 2007), and *Fundamentals of Performance Evaluation of Computer and Telecommunications Systems* (Wiley 2003). He served also as editor or guest editor of numerous international journals.

Obaidat has served as distinguished speaker/visitor of IEEE Computer Society, ACM and SCS distinguished Lecturer. He served as the Scientific Advisor for the World Bank/UN Digital Inclusion Workshop. He was member of the board of directors of the Society for Computer Simulation International. He served as Vice President of Conferences of the Society for Modeling and Simulation International SCS and as SCS Vice President of Membership. Currently, He is the Senior Vice President of SCS. His research interests are: wireless communications and networks, telecommunications and Networking systems, security of network, information and computer systems, security of e-based systems, performance evaluation of computer systems, algorithms and networks, high performance and parallel computing/computers, applied neural networks and pattern recognition, adaptive learning and speech processing.

Recently, Prof. Obaidat has been awarded a Nokia Research Fellowship and the distinguished Fulbright Scholar Award. Prof. Obaidat is a Fellow of the Society for Modeling and Simulation International SCS, and a Fellow of the Institute of Electrical and Electronics Engineers (IEEE).



Trends in complex SoC Design: From technology variability to multiprocessor architectures

Didier Lattard, CEA-LETI, France



Didier Lattard was born in Saint Marcellin, France, in 1963. He received his Ph.D. degree in Microelectronics from the National Polytechnic Institute of Grenoble, France, in 1989.

In 1990, he joined the CEA-LETI laboratory in the Center for Innovation in micro & nanotechnology (MINATEC), Grenoble. He was involved in the design of image and baseband processing circuits as senior R&D engineer and project leader. From 2003 to 2006, he led the development of the FAUST NoC-based telecom platform. Since 2006, he has been in charge of new projects in imaging and high-performance computing applications. He has published 29 papers in books, refereed journals and conferences. He holds 17 patents in the fields of baseband processing and NoC architectures.

Low-Voltage Limitations and Challenges of
Memory-Rich Nano-Scale CMOS LSIs

Kiyoo Itoh, Hitachi, Japan



KIYOO ITOH received the B.S. and Ph.D. Degrees in Electrical Engineering from Tohoku University, Japan, in 1963 and 1976. He is currently a Hitachi Fellow. He was a Visiting MacKay Lecturer at U.C. Berkeley, a Visiting Professor at the U of Waterloo, and a Consulting Professor at Stanford U. He was a Member of the IEEE Fellow Committee, and an elected AdCom Member of IEEE Solid-State Circuits Society. He is a Distinguished Lecturer of the IEEE Solid-state Circuits Society. Since 1972 he has led RAM circuit technology at Hitachi Ltd: He was the lead designer of the first prototype for eight generations of Hitachi DRAMs ranging from 4Kb to 64Mb. In the course of the developments he invented in 1974 the concept of folded data-line architecture, which uses a pair of balanced data lines to eliminate various noise components, and presented the architecture for a 64-Kb DRAM at the 1980 ISSCC. Since that time, this architecture has been adopted for nearly all DRAM chips since produced. He went on to develop key DRAM devices, circuits, and architectures such as the triple-well structure, on-chip voltage down-converters enabling the aging (burn-in) stress test, and low-power high-speed PMOS word driver and multi-divided data-line architecture. As early as 1988, he initiated circuit inventions and developments to reduce subthreshold current of MOSFETs even for the active mode, which is highlighted today in low-voltage CMOS LSI design. Typical examples of the reduction circuits are multi-threshold (V_t) CMOS logic, various gate-source (self) back-biasing schemes, and power switch that we take for granted today. He holds over 420 patents in Japan and US. He authored four books and three book chapters on memory designs, and contributed over 130 technical papers and presentations. Dr. Itoh has won many honors: IEEE Paul Rappaport Award, the Best Paper Award of ESSCIRC90, IEEE Solid-State Circuits Award, and IEEE Jun-ichi Nishizawa Medal. He is an IEEE Fellow. In Japan, his awards include the National Invention Award (Prize of the Patent Attorney's Association of Japan) in 1989, the Commendation by the Minister of State for Science and Technology (Person of Scientific and Technological Merits) in 1997, and the National Medal of Honor with Purple Ribbon in 2000.

Wednesday, December 12, 2007, 08:30 - 08:45

A0L-A Opening Remarks

Place: Auditorium

Wednesday, December 12, 2007, 08:45 - 09:30

A1L-A Keynote: Andreas G. Andreou

Place: Auditorium

Chair: Mohammed Ismail; *Ohio State U., USA*

Microsystems Engineering from Nano to Micro and Macro
Andreas G. Andreou, *Johns Hopkins U.*

Wednesday, December 12, 2007, 09:30 - 10:15

A2L-A Keynote: Giovanni DeMicheli

Place: Auditorium

Chair: Amara Amara; *ISEP, France*

New Design Paradigms: New Architectures for New Technologies
Giovanni Demicheli, *Ecole Polytechnique Federale de Lausanne*

Wednesday, December 12, 2007, 10:15 - 10:40

A3P-G Advanced technologies

Place: Poster Area 1

Chair: Zouhair Guennoun; *EMI, Morocco*

Design of a Millimetre Synthetic Aperture Radar (SAR) Onboard UAV's
Raquel Ruiz Saldaña, Félix Pérez Martínez, *Polytechnic U. of Madrid, Spain*

Microelectronic Magnetic Flux Sensor for Hearing Aid Application
Crystal Kenney, David Kotecki, *U. of Maine*

An Integrated Laser Radar Receiver Channel with Wide Dynamic Range
Jan Nissinen, Juha Kostamovaara, *U. of Oulu*

VCSEL Device Modeling and Parameter Extraction Technique
Kyriaki Minoglou, Georgios Halkias, *NCSR-Demokritos*; Efsthios Kyriakis-Bitaros, *TEI of Pireaus*; Dimitrios Syvridis, Aggeliki Arapogianni, *U. of Athens*

On-Chip High Voltage Generation with Standard Process for MEMS
Ming Zhang, Nicolas Llaser, *U. of Paris XI*

A 12-Channel 60-Gb/S Transimpedance Amplifier and Limiting Amplifier Array for OPCB Applications
Wonseok Oh, *Korea Electronics Technology Institute*; Kangyeob Park, *U. of Yonsei*

Low-Gain-Wide-Range 2.4-GHz Phase Locked Loop
Wenceslas Rahajandraibe, Lakhdar Zaid, Vincent Cheynet de Beaupré, Julien Roche, *U. of Provence*

HW/SW FPGA Architecture for a Flexible Motion Estimation

Ahmed Ben Atitallah, *National Engineering School of Sfax and U. Bordeaux 1*; Patrice Kadionik, *U. Bordeaux 1*; Nouri Masmoudi, *LETI-ENIS*; Hervé Levi, *U. Bordeaux 1*

Importance Sampling Applied to an Optical DS-CDMA System

Amel Farhat, *Ecole Nationale d'Ingénieurs de Tunis*; Mourad Menif, *Ecole Supérieure des Communications*; Catherine Lepers, *U. de Lille I*; Houria Rezig, *Ecole Nationale d'Ingénieurs de Tunis*; Philippe Gallion, *Ecole Nationale Supérieure des Télécommunications*

Low Cost Library for Preprocessing of Digital Speech Signals

Daniella Silva, Elmar Melcher, Joseana Fechine, Benedito Aguiar Neto, *U. Federal de Campina Grande*

Digital Measurement Technique for Capacitance Variation Detection on Integrated Circuit I/Os

Yves Blaquièrre, *U. du Québec à Montréal*; Yvon Savaria, Jaouad El Fouladi, *École Polytechnique*

A Low Drift, Low Noise Detection IC Applied to MEMS Gyros

Raphael Levy, Antoine Dupret, Hervé Mathias, Fabien Parrain, *U. Paris Sud*; Jean Guerard, *ONERA*

A New Gas Recognition Technique Using on Chip Sensor Array Measurements

Farid Flitti, Bin Guo, Aicha Beya Far, Amine Bermak, *Hong Kong U. of Science and Technology*

PSpice Modelling Diffraction Effects in Pulse Echo Ultrasonic System

Noureddine Aouzale, *Electrical Systems and Telecommunication Laboratory*; Ahmed Chitnalah, Hicham Jakjoud, *Electrical Systems and Telecommunication Laboratory Faculty of Science and Technology of Marrakech*; Djilali Kourtiche, *Nancy U. - U. Henri Poincaré*

Modeling and Simulation of Photovoltaic Panel Based on Artificial Neural Networks and VHDL-Language

H. Mekki, Adel Mellit, H. Salhi, B. Khaled, *Blida U.*

A4L-A SPECIAL SESSION: Implantable Devices

Place: Auditorium

Chair: Mohamad Sawan; *École Polytechnique, Canada*

Towards a Brain-Machine-Brain Interface (BMBI) for Anatomical Rewiring of Cortical Circuitry

Meysam Azin, Pedram Mohseni, *Case Western Reserve U.*

An ENG Amplifier with Passive EMG Neutralization

Andreas Demosthenous, Ioannis Pachnis, Mohamad Rahal, Dai Jiang, Nick Donaldson, *U. College London*

Design and Optimization of Printed Spiral Coils for Efficient Inductive Power Transmission

Uei-Ming Jow, Maysam Ghovanloo, *Georgia Institute of Technology*

Low-Noise ASIC and New Layout of Multipolar Electrode for Both High ENG Selectivity and Parasitic Signal Rejection

Serge Bernard, *LIRMM - CNRS/U. Montpellier*; Lionel Gouyet, Guy Cathebras, Fabien Soulier, *LIRMM - UMII*; David Guiraud, *LIRMM - INRIA*; Yves Bertrand, *LIRMM -UMII*

Design Practice of Power-Oriented Integrated Circuits for Biomedical Implant Systems

Zhihua Wang, Songping Mai, Chun Zhang, Hong Chen, *Tsinghua U.*

A4L-B Analog EDA

Place: Room 1

Chair: Sergio Bampi; *Federal Univ Rio Grande do Sul, Brazil*

New Analog Test Metrics Based on Probabilistic and Deterministic Combination Approaches

Abdessatar Abderrahman, *Ecole polytechnique de Montréal*; Mohamad Sawan, Yvon Savaria, Abdelhakim Khouas, *École Polytechnique de Montréal*

Effective Spice Analysis of Switched Capacitor DC-DC Converters

Dalibor Bišek, *U. of Defence/Brno U. of Technology*; Viera Biolková, Zdenek Kolka, *Brno U. of Technology*

Behavioural and Electrothermal Modelling of the IGBT for Circuits Simulation

Elmostafa Elwarraki, *U. Cadi Ayyad*; Abderrafia Sabir, *Hassan II U.*

Stochastic Behavior of a CMOS Inverter

Peng Xu, *U. of Maryland*; Pamela Abshire, *Electrical and Computer Engineering, Institute for Systems Research, U. of Maryland*

Synchronization Analysis of a Switched Oscillator

Pere Palà-Schönwälder, *U. Politècnica de Catalunya-Technical U. of Catalonia*; Francisco Del-Águila-López, F. Xavier Moncunill-Geniz, Rosa Giralt-Mas, *U. Politècnica de Catalunya*

A4L-C Wireless Networks

Place: Room 2

Chair: Hervé Barthelemy; *L2MP, France*
Meng-Ting Tsai; *Industrial Technology Research Institute, Taiwan*

Study of Mac Effect on Load-Balanced Short-Path Routing Algorithm in Wireless Networks
Hossam Fahmy, Salma Ghoneim, *Ain Shams U.*

A Bandwidth Allocation Algorithm for Multiuser OFDM Systems and its Efficient Implementation

Nikolaos Papandreou, Theodore Antonakopoulos, *U. of Patras*

Comparison of Propagation Models Accuracy for WiMAX on 3.5 GHz

Josip Milanovic, *Croatian Telecommunications Agency*; Snjezana Rimac-Drlje, *Univeristy of Osijek*;
Krunoslav Bejuk, *Croatian Telecommunications Agency*

Throughput Enhancement in Wireless Slotted ALOHA via Collision Processing

Nejah Missaoui, Ines Kammoun, *National Engineering School of Sfax*; Mohamed Siala, *Ecole Supérieure des Communications de Tunis*

A4L-D Classifiers

Place: Room 3

Chair: Majid Ahmadi; *Univ of Windsor, Canada*

Optimal Frequency SSD Matching Using Cosine Kernel

Fedwa Essannouni, *GSCMLRIT*; Rachid Oulad Haj Thami, *WIM*; Driss Aboutajdine, *LRIT-GSCM*,
U. Mohamed V Rabat; Ahmed Salam, *LMPA*

A New Method for the Design of K-Class Bayes Classifiers

Roghayeh Doost, Mohammad Rahmati, Abolghasem Sayyadian, *Amirkabir U. of Technology*;
Hossein Shamsi, *Khajeh Nasir Toosi U.*

Synthesis of Classification Supervised Algorithms for Players Identification During a Sports Meeting

Mourad Moussa Jlassi, Ali Douik, *Ecole Nationale d'Ingénieurs de Monastir*; Tahar Battikh,
Mohamed Annabi, *Ecole Supérieure des Sciences et Techniques de Tunis*

Analysis of EEG Using Principal Component Approach

Yarlagadda Padmasai, *VNR Vignana Jyothi Institute of Engineering and Technology(VNRVJIET)*;
Kakarla Subbarao, *U. College of Engg. Osmania U.*; C Raghavendra Rao, *Hyderabad Central U.*; S Sita Jayalakshmi, *NIMS*

A Fast Algorithm Including Linear Prediction Method to Decode Both DTMF and Clip Signals

Mohamed Moughit, Abdelmajid Badri, Aicha Sahel, *Faculté des Sciences et Techniques, Mohamédia*

A4L-E High Performance Digital Circuits

Place: Room 4

Chair: Ricardo Reis; *UFRRGS, Brazil*

On the Design of Scalable Massively Parallel CRC Circuits

Konstantin Septinus, *Leibniz U. of Hannover*; Thuyen Le, Ulrich Mayer, *IBM Deutschland Entwicklung GmbH*; Peter Pirsch, *Leibniz U. of Hannover*

High Performance 16K, 64K, 256K Complex Points VLSI Systolic FFT Architectures

Konstantinos Manolopoulos, Konstantinos Nakos, *NKUA*; Dionysios Reisis, *National and Kapodistrian U. of Athens*; Nikolaos Vlassopoulos, *NKUA*; Vassilios Chouliaras, *Loughborough U.*

High Throughput Architecture for Forward Transforms Module of H.264/AVC Video Coding Standard

Roger Porto, Marcelo Porto, Sergio Bampi, *Federal U. of Rio Grande do Sul*; Luciano Agostini, *Federal U. of Pelotas*

Datapath Delay Distributions for Data/Instruction Against PVT Variations in 90nm CMOS

Makoto Ikeda, Ken Ishii, Taku Sogabe, Kunihiro Asada, *U. of Tokyo*

Nonoverlapping Cuspid-Pulsed Flip-Flop

Min-Su Kim, *SungKyunKwan U. and Samsung Electronics*; Bai-Sun Kong, Chil-Gee Lee, *SungKyunKwan U.*; Tae-Hyung Kim, Sung Bae Park, Young-Hyun Jun, *Samsung Electronics*

A4L-F Design Optimizations and Estimation

Place: Room 5

Chair: Guy Bois; *École Polytechnique, Canada*
Mohsine Eleuldj; *EMI, Morocco*

Design and Optimization of IIR Digital Filters with Non-Standard Characteristics Using Particle Swarm Optimization Algorithm

Adam Slowik, Michal Bialko, *Technical U. of Koszalin*

Accurate Delay Estimation in the Presence of Coupling Noise Using Complete Waveform Accuracy

Jingye Xu, *U. of Illinois at Chicago*; Masud Chowdhury, *University of Illinois at Chicago*

Systematic Offset Detection and Evaluation Using Hierarchical Graph-Based Sizing and Biasing

Ramy Iskander, Marie-Minerve Louërat, *U. Pierre et Marie Curie*; Andreas Kaiser, *IEMN*

Cooling Management of a Protruding Electronic Components by Using a Phase Change Material Heat Sink

Mustapha Faraji, *U. Cadi Ayyad*; Hamid El Qarnia, *U. Cadi Ayyad*

FPGA-Based Implementation of Ram with Asymmetric Port Widths for Run-Time Reconfiguration

Raouf Senhadji-Navarro, Ignacio García-Vargas, Gabriel Jiménez-Moreno, Antón Civit-Balcells, *Universidad de Sevilla*

Wednesday, December 12, 2007, 13:40 - 14:25

A5L-A Keynote: Magdy Bayoumi

Place: Auditorium

Chair: Bozena Kaminska; *Simon Fraser Univ, Canada*

New Wireless Sensors Networks: The Art of Integration
Magdy Bayoumi, *U. of Louisiana at Lafayette*

Wednesday, December 12, 2007, 14:30 - 16:00

A6L-A SPECIAL SESSION: Emerging Technologies

Place: Auditorium

Chair: Marc Belleville; *CEA-LETI, France*

FinFET Technology for Analog and RF Circuits

Bertrand Parvais, *IMEC*; Vaidy Subramanian, *IMEC and Katholieke Universiteit Leuven*;
Abdelkarim Mercha, Morin Dehan, *IMEC*; Piet Wambacq, *IMEC and Vrije Universiteit
Brussels*; Willy Sanssen, *Katholieke Universiteit Leuven*; Guido Groeseneken, Stefaan
Decoutere, *IMEC*

Advances in Multi-Gate MOSFET Circuit Design

Michael Fulde, *Technical U. Munich*; Klaus von Arnim, Christian Pacha, Florian Bauer, Christian
Russ, Domagoj Siprak, *Infineon Technologies*; Wade Xiong, A. Marshall, Rinn Cleavelin;
Texas Instruments; Klaus Schroefer, *Infineon Technologies*; Doris Schmitt-Landsiedel,
Technical U. Munich; Gerhard Knoblinger, *Infineon Technologies*

CMOS/Magnetic Hybrid Architectures

Guillaume Prenat, Mourad El Baraji, Wei Guo, Ricardo Sousa, Liliana Buda-Prejbeanu, Bernard
Dieny, *Spintec Laboratory CEA/CNRS*; Virgile Javerliac, Jean-Pierre Nozieres, *Crocus-
Technology*; Weisheng Zhao; ; Eric Belhaire, *U. Paris Sud*

Ultra-Fine Grain reconfigurability Using CNTFETs

Ian O'Connor, Junchen Liu, David Navarro, Ilham Hassoune, Stéphane Burignat, Frédéric Gaffiot,
Ecole Centrale de Lyon - INL

**Analog Design Considerations for Independently Driven Double Gate MOSfets and their
Application in a Low-Voltage OTA**

Philippe Freitas, Gérard Billiot, *CEA LETI - MINATEC*; Hervé Lapuyade, J.B. Begueret, *IMS - IXL
Laboratory, France*

A6L-B Charge Pumps and Switches

Place: Room 1

Chair: Pejcinovic Branimir; *Portland State Univ, USA*

A Dual Phase Charge Pump with Compact Size

Chun-Yu Hsieh, Po-Chin Fan, Ke-Horng Chen, *National Chiao Tung U.*

**A New Architecture for Charge Pump Circuit Without Suffering Gate-Oxide Reliability in
Low-Voltage CMOS Processes**

Tzu-Ming Wang, Wan-Yi Sheng, *National Chung-Tung U.*; Ming-Dou Ker, *National Chiao-Tung U.*

Time-Shifted CDS Enhancement of Comparator-Based MDAC for Pipelined ADC Applications

Omid Rajaei, Nima Maghari, Un-Ku Moon, *Oregon State U.*

An Automated Design Methodology for Charge Pump Circuits

Hassen Aziza, *L2MP*; Emmanuel Bergeret, *STMicroelectronics*; Annie Perez, *L2MP*

Design of Improved Rail-to-Rail Low-Distortion and Low-Stress Switches in Advanced CMOS Technologies

Acacio Galhardo, *Instituto Superior de Engenharia de Lisboa*; João Goes, Nuno Paulino, *U. Nova de Lisboa*

A6L-C Analog to Digital Converters

Place: Room 2

Chair: Pieter Harpe; *Eindhoven Univ of Technology, Netherlands*

Analysis and Performance Comparison of a Cascade 3-1 Delta-Sigma Topology

Koen Cornelissens, Michiel Steyaert, *Katholieke Universiteit Leuven*

Structural DFT Approach on Folded ADCs

Roman Mozuelos, Yolanda Lechuga, Mar Martinez, Salvador Bracho, *U. of Cantabria*

A Sigma-Delta Converter with Adjustable Tradeoff Between Resolution and Consumption

Philippe Benabes, Sylvie Guessab, *SUPELEC*

Design Considerations for Stochastic Analog-to-Digital Conversion

Skyler Weaver, *Oregon State U.*; Daniel Knierim, Roland Wanzneried, *Tektronix, Inc.*; Un-Ku Moon, *Oregon State U.*

A Cognitive Digitally-Enhanced Radio Delta Sigma ADC

Pukar Malla, *Cornell U.*; Hasnain Lakdawala, *Intel Corporation*; Krishnamurthy Soumyanath, *Intel Corporation*; Kevin Kornegay, *Georgia Institute of Technology*

A6L-D Digital Filter Design I

Place: Room 3

Chair: Mohammed Al-Mualla; *Etisalat U. College, UAE*

Design of ANSI S1.11 Filter Bank for Digital Hearing Aids

Yu-Ting Kuo, Tay-Jyi Lin, Yueh-Tai Li, Wei-Han Chang, Chih-Wei Liu, *National Chiao Tung U.*; Shuenn-Tsong Young, *National Yang-Ming U.*

Common Subexpression Elimination for Digital Filters Using Genetic Algorithm

Payman Samadi, Majid Ahmadi, *U. of Windsor*

A New Modified Comb-Rotated Sinc (RS) Decimator with Improved Magnitude Response

Gordana Jovanovic Dolecek, *Institute INAOE*

Gaussian Shaped Multiband FIR and IIR 2D Filters

Radu Matei, *Technical U. 'Gh.Asachi'*

Designing FIR Digital Filters with the Specified Maximum Group Delay Errors

Yasunori Sugita, *Nagaoka U. of Technology*; Naoyuki Aikawa, *Nihon U.*; Toshinori Yoshikawa, *Nagaoka U. of Technology*

A6L-E Power Amplifiers and Circuits

Place: Room 4

Chair: Joseph Micallef; *Univ of Malta*

RF Power Amplifier with Cartesian Feedback for Tetra(TM) Modulation

Narendra Kumar, *Motorola Technology*; Lokesh Anand, *Univesity Science Malaysia*; Pragash Sangaran, Subramaniam Anbalagan, *Motorola Technology*; Georg Boeck, *Berlin U. of Technology*

Impedance Adjustment for Constant Efficiency Power Amplifier Applying Stage Bypass Method

Narendra Kumar, *Motorola Technology*; Lokesh Anand, *Univesity Science Malaysia*; Pragash Sangaran, Subramaniam Anbalagan, *Motorola Technology*; Georg Boeck, *Berlin U. of Technology*

A FET Propagation Effects

Moez Balti, A. Samet, *SysCom de l'ENIT*; D. Pasquet, *Laboratoire ECIME de l'ENSEA*

Investigation of Efficiency Vs. Linearity Trade-Offs in LINC Amplifiers for Varying Outphasing Combiner Reactances

Walid Hamdane, Mohamad El-Asmar, A Birafane, A. B. Kouki, *Ecole de Technologie Superieure*

Exact Analytical Expressions of Graetz Bridge Currents and Voltages Using Lambert W Function

El Mahdi Assaid, *Faculty of Sciences, El Jadida*; El Mustapha Feddi, *ENSET Mohammedia*; M'Hamed El Aydi, *C.P.R. El Jadida*

A6L-F Optimizations in Simulation, Modeling and Verification

Place: Room 5

Chair: Malgorzata Chrzanowska-Jeske; *Portland State U., USA*
Michal Bialko; *Technical U. of Koszalin, Poland*

Automatic Optimization Techniques for Formal Verification of Asynchronous Circuits

Menouer Boubekeur, *U. College Cork*; Michel Schellekens, *UCC, CEOL Centre*

Automatic Generation of VHDL Code for Self-Timed Circuits from Simulink Specifications

Maurizio Tranchero, Leonardo Reyneri, *Politecnico di Torino*

Simulation of Voice Processing Applications Through VLIW DSP Architectures

Naser Sedaghati, Mahdi Nazm Bojnordi, Amin Farmahini-Farahani, *U. of Tehran*; Mahmoud Mousavinezhad, *Iran Telecommunication Research Center*; Sied Mehdi Fakhraie, *U. of Tehran*

Acceleration for Heterogeneous Systems Cosimulation

Mathieu Dubois, *U. de Montréal/Diro*; El Mostapha Aboulhamid, *U. de Montréal*; Frédéric Rousseau, *Laboratoire TIMA*

Rapid Prototyping IP for Autocorrelation Computation

Fatma Sayadi, Mohamed Atri, Rached Tourki, *Faculté des Sciences de Monastir*

A7P-G Digital Circuits, DSP and Multimedia

Place: Poster Area 1

Chair: Zouhair Guennoun; EMI, Morocco

A Simplified Method for IIR Filter Design with Quasi-Equiripple Passband and Least-Squares Stopband

Jacek Konopacki, Katarzyna Moscinska, *Silesian U. of Technology*

Reducing Leakage Power in Fixed Coefficient Arithmetic

Peter Nilsson, *Lund U.*

Mathematical Functions Based Watermarking for IPP

Bertrand Le Gal, Lilian Bossuet, Dominique Dallet, *U. of Bordeaux 1*

HLS Design Flow for the Synthesis of Multimode Systems Under Multiple Constraints

Bertrand Le Gal, Lilian Bossuet, *U. of Bordeaux 1*; Shafqat Khan, Emmanuel Casseau, *U. of RENNES 1*

Orthogonal Schur-Type Solution of the Nonlinear Echo-Cancelling Problem

Pawel Biernacki, *U. of Technology Wroclaw*

A Transmission Line Modelling VLSI Processor Designed with a Novel Electronic System Level Methodology

Vassilios Chouliaras, James Flint, *Loughborough U.*; Yibin Li, *Queens U., Belfast*

On Deratings to Refine System-Level Failure Rate Estimations

Christophe Smekens, Régis Leveugle, *TIMA Laboratory*

A Masking Model of HVS for Image Watermaking in the DCT Domain

Samia Belkacem, Zohir Dibi, *U. of Batna*; Ahmed Bouridane, *Queens U., Belfast*

Automatic Face Tracking and Identity Verification

Leila Essannouni, *Faculté des Sciences, Rabat*; El Hassan Ibn Elhaj, *Institut National des Postes et Telecommunications*; Driss Aboutajdine, *LRIT-GSCM, U. Mohamed V Rabat*

Evaluation of All-Pass Reverberators

Marina Dana Topa, Norbert Toma, Victor Popescu, Vasile Topa, *Technical U. of Cluj-Napoca*

Color Image Watermarking Based on Chaotic Map

Samia Belkacem, Zohir Dibi, *U. of Batna*; Ahmed Bouridane, Moussadek Laadjel, *Queens U., Belfast*

Color Images Watermarking by Means of Independent Component Analysis

Moilim Amir, *LRIT-Faculté des Sciences, Rabat*; Abdellah Adib, *Institut Scientifique, Rabat*; Driss Aboutajdine, *LRIT-GSCM, U. Mohamed V Rabat*

Support Vector Machine for Internet Traffic Identification

Amina El Gonnouni, *U. Abdelmalek Essaadi-Tangier*; Soufiane El Jelali, *U. Carlos III*; Jilali Antari, *U. Cadi Ayyad*; Abdelouahid Lyhyaoui, *Abdelmalek Essaadi U.*

Linear Feedback Control of Multi DC Bus Link Voltages of Multilevel NPC VSI Cascade

Abdelaziz Talha, Dalila Beriber, *U. of Science and Technology Houari Boumediene*

A8L-A Analog Design

Place: Auditorium

Chair: Mark Zwolinski; *U.of Southampton , U.K*
Ke-Horng Chen; *National Chiao Tung Univ, Taiwan*

A CMOS High-Q LC Eight-Path Bandpass Filter for Wireless Broadband Applications

Ahmed El Oualkadi, *MSESY-ENSAM, Morocco*; Jean-Marie Paillot, *LAIL-ESIP, France*; Said Belkouch, *MSESY-ENSAM, Morocco*; Denis Flandre, *U. Catholique de Louvain*

A Phase Interpolator for Sub-1V and High Frequency for Clock and Data Recovery

Kuo-Hsing Cheng, Pei-Kai Tseng, Yu-Lung Lo, *National Central U.*

A Wake-Up Circuit with Temperature Compensated Clock in 1.2V-0.13 μ m CMOS Technology

Angel Dieguez, Anna Arbat, Andreu Sanuy, Raimon Casanova, Marc Rossinyol, Josep Samitier, *U. of Barcelona*

Testing Low-Resolution DACs Using the Generalized Morse Sequence As Stimulus Sequence for Cancelling DC Drift

Jan Schat, *NXP Semiconductors*

Design and Use of FR-4 CBCPW Lines in Test Fixtures for SMD Components

Branimir Pejcinovic, *Portland State U.*; Vladimir Ceperic, Adrijan Baric, *U. of Zagreb*

A8L-B Current Conveyors and Current Mode Circuits

Place: Room 1

Chair: Bilal Manai; *ATMEL Rousset, France*
Robert C. Chang; *National Chung-Hsing Univ, Taiwan*

Synthesis of CCII and Design of Simulated CCII Based Floating Inductances

Mourad Fakhfakh, Mourad Loulou, *National Engineering School of Sfax*; Esteban Tlelo-Cuautle, *Institute INAOE*

Simplified BiCMOS Current Controlled Conveyor

Mustapha Alami, *INPT, Rabat*; Alain Fabre, *Ecole Nationale Supérieure d'Electronique, d'Informatique et de Radiocommunications de Bordeaux*; Jaadoud Abdelkader, *Faculté des sciences Ain Chock*; Abdelkader Touhami, *Laboratoire sciences des matériaux, électronique et systèmes industriels, Faculté des sciences Ain Ch*

A New High Frequency Second Generation Current Conveyor Based Chaos Generator

Achwek Ben Saied, Samir Ben Salem, Moez Feki, Dorra Masmoudi, *U. of Sfax*

Low Voltage Programmable Double-Gate MOSFETs Current Mirror and its Application As Programmable-Gain Current Amplifier

Hesham Hamed, *El-Minia U.*; Savas Kaya, *Ohio U.*

A8L-C Sensor Applications

Place: Room 2

Chair: [Ali Hellany; Univ of Western Sydney, Australia](#)
[Masahiro Sasaki; U. of Tokyo, Japan](#)

Smart-Pixel Array for Imaging Sensors

Andre Fernandes, Jose Rocha, Graca Minas, *U. of Minho*

Wireless Sensor for Intravenous Dripping Detection

Paul Bustamante, Unai Bilbao, N. Guarretxena, G. Solas, *U. of Navarra*

Electro-Enzymatic Glucose Sensor Using Hybrid Polymer Fabrication Process

Jasbir Patel, Bozena Kaminska, Bonnie Gray, Byron Gates, *Simon Fraser U.*

Curve Reconstruction via a Ribbon of Sensors

Nathalie Sprynski, Dominique David, *CEA LETI - MINATEC*; Bernard Lacolle, Luc Biard, *U. Joseph Fourier*

Comb Types Channel Estimation in Multiple Access OFDM System

Samah Mustafa, Sangar Kadr, *Salahaddin U.*

A8L-D Modeling and Design of Heterogeneous Circuits and Systems

Place: Room 3

Chair: [Aggeliki Arapogianni; Univ of Athens, Greece](#)
[Lahbib Zenkouar; EMI, Morocco](#)

Numerical Study of supercontinuum Generation in Photonic Crystal Fiber

Rim Cherif, Mourad Zghal, *Ecole Supérieure des Communications de Tunis*

Behavioral Modeling of the Ph-ISFET Temperature Influence

Salah Eddine Naimi, Bekkay Hajji, *Mohammed 1st U.*; I. Humenyuk, J. Launay, P. Temple-Boyer, *U. of Toulouse*

On-Chip Integrated Optical Sensors for Fluorescence Detection of Cancer Tissue: Application to Capsule Endoscopy

Rosana Dias, Jose Correia, Graca Minas, *U. of Minho*

Towards the High-Level Design of Optical Networks on-Chip. Formalization of Opto-Electrical Interfaces

Matthieu Briere, Luiza Gheorghe, *Ecole Polytechnique Montreal*; Gabriela Nicolescu, *École Polytechnique de Montréal*; Ian O'Connor, *Ecole Centrale de Lyon - INL*; Gabriel Wainer, *Carleton U.*

A8L-E Power Issues in Digital Circuits

Place: Room 4

Chair: Massimo Alioto; *U. of Siena, Italy*
Jinkeun Hong; *Baekseok U., Korea*

A Simple and Accurate Model of Input Capacitance for Power Estimation in CMOS Logic
Massimo Alioto, *U. of Siena*

Testing of Level Shifters in Multiple Voltage Designs
Noohul Basheer Zain Ali, Mark Zwolinski, Bashir M Al-Hashimi, *U. of Southampton*

A Scan Flip-Flop for Low-Power Scan Operation
Yiorgos Tsiatouhas, *U. of Ioannina*; Angela Arapoyanni, Dionisis Skias, *U. of Athens*

Low Power and Stable FinFET SRAM with Static Independent Gate Bias for Enhanced Integration Density
Sherif Tawfik, Volkan Kursun, *U. of Wisconsin, Madison*

A8L-F Design using Parallel Architectures

Place: Room 5

Chair: Ismaïl Assayad; *VERIMAG, France*
Lars Wanhammar; *Linköping U., Sweden*

A Cost-Effective Parallel Architecture for the CodeRAKE Receiver
Mazen Youssef, Fabrice Monteiro, Abbas Dandache, Camille Diou, *U. Paul Verlaine-Metz*

Comparison of VLSI Architectures for a WLAN OFDM Transmitter with Interpolation Filters
Pavlos Kolovos, Eleni Fotopoulou, Thanos Stouraitis, *U. of Patras*

Design of a Telecommand and Telemetry System for Use on Board a Nanosatellite
Adnane Addaim, Abdelhak Kherras, *CRÉS, Mohammadia School of Engineers*; El Bachir Zantou, *CRÉS*

Robust Predictive Control Using a GOBF Model for MISO Systems
Ali Douik, Jalel Ghabi, Messaoud Hassani, *Ecole Nationale d'Ingénieurs de Monastir*

Solar Grid-Connected Three-Phase System with Active and Reactive Power Control and Input Voltage Clamped
Mateus Felzke Schonardie, Denizar Cruz Martins, *Federal U. of Santa Catarina and Power Electronics Institute*

Wednesday, December 12, 2007, 18:00 - 19:00

Panel Discussion: Globalization in the domain of circuits and Systems: Impacts, costs and benefits

Place: Auditorium

Chair: Pierre Paulin, *STMicroelectronics, Canada*

Thursday, December 13, 2007, 08:30 - 09:15

B1L-A Keynote: Mohammad S. Obaidat

Place: Auditorium

Chair: Abdelhakim Hafid; *Univ de Montréal, Canada*

Trends and Challenges in Wireless Systems
Mohammad Obaidat, *Monmouth U.*

Thursday, December 13, 2007, 09:20 - 10:50

B2L-A Design and Applications of Heterogeneous Systems

Place: Auditorium

Chair: Rainer Wohlgenannt; *Austrian Research Centers, Austria*
Noureddine ElAlami; *EMI, Morocco*

Electro-Optical Synthesis of a WDM PHASAR: Study the Tunability and Determination of the Command Voltage
Amal Sabbar, Abderraouf Aboudou, Abdellatif Hamdoun, *U. Hassan II*

Design and Test of a Digital System Based on a CMOS 0.35 μ m Logarithmic Pixel for Pulsed Laser Optical Detection
Ivan Bernat Ubiaga, Marta Padilla, Mauricio Moreno, Angel Dieguez, Josep Samitier, *U. of Barcelona*

A Full-Custom Mixed-Signal CMOS Front-End Readout Chip for High Efficiency Small Animal PET Imaging
Ndeye Awa Mbow, Patrick Bard, David Brasse, Claude Colledani, C. Fuchs, Jean-Louis Guyonnet, Christine Hu-Guo, Bernard Humbert, Nicolas Ollivier-Henry; ; Yann Hu, *Institut Pluridisciplinaire Hubert Curien*

A Navigation System for a Wheelchair User Based on a Multi-Modal Design
Mohamed Fezari, Hamza Attoui, *U. of Annaba*

PI-Fuzzy Controller Conception with Design Pattern Based Approach
Yassine Manai, Joseph Haggège, Mohamed Benrejeb, *Ecole Nationale d'Ingénieurs de Tunis*

B2L-B Oscillators and Amplifiers

Place: Room 1

Chair: Mourad Loulou; *National Engineering School of Sfax, Tunisia*
Sylvie Renaud; *U. of Bordeaux 1, France*

CMOS Inverters Based High Frequency Voltage Controlled Sinusoidal Oscillator
Hervé Barthélemy, Sylvain Bourdel, Jean Gaubert, Marc Battista, *L2MP*

Design and Analysis of Noise Tolerant Ring Oscillators Using Maneatis Delay Cells
Josh Carnes, Igor Vytyaz, Pavan Kumar Hanumolu, Kartikeya Mayaram, Un-Ku Moon, *Oregon State U.*

A High Swing Low Power CMOS Differential Voltage-Controlled Ring Oscillator
Luciano de Paula, Sergio Bampi, Eric Fabris, Altamiro Susin, *Federal U. of Rio Grande do Sul*

Capacitor-Multiplier Frequency Compensation for Low-Power Multistage Amplifiers
Zu-Shu Yan, *Beijing Microelectronics Technology Institute*; Lianguo Shen, *Peking U.*; Yuan-Fu Zhao, Suge Yue, *Beijing Microelectronics Technology Institute*

Band Pass Pseudo Floating-Gate Amplifier
Yngvar Berg, *U. of Oslo*; Mehdi Azadmehr, *Vestfold U. College*; Omid Mirmotahari, Snorre Aunet, *U. of Oslo*

B2L-C Algorithms and Communication Systems

Place: Room 2

Chair: Panayiotis Savvopoulos; *Univ of Patras, Greece*
Dalila Chiadmi, *EMI, Morocco*

On the Use of Artificial Intelligence for MAI Cancellation in DS/CDMA Over Rayleigh Fading Channel with Power Control Error

Younes Jabrane, Radouane Iqdour, Brahim Ait Es Said, *U. Cadi Ayyad*; Najib Naja, *INPT*

Hierarchical Sequential Detection in the Context of Dynamic Spectrum Access for Cognitive Radios

Nikhil Kundargi, Ahmed Tewfik, *U. of Minnesota*

DACA: Dynamic Advanced Clustering Algorithm for Sensor Networks

Hamidreza Alipour, *Shahid Beheshti U.*; Maghsoud Abbaspour, *School of Computer Science, Tehran*; Mostafa Esmaeili, Hamed Mousavi, Hamed Shahhoseini, *Shahid Beheshti U., Tehran*

3.5-Gb/S Extended Frequency Range Wave-Pipeline PRBS Generator in 0.18- μ m CMOS

Masahiro Sasaki, Makoto Ikeda, Kunihiko Asada, *U. of Tokyo*

A Comparative Study for Real Time Scheduling

Sahla Masmoudi, *Ecole Nationale des Sciences de l'informatique*; Leila Azouz Saidane, *U. of Manouba*

B2L-D Image Processing

Place: Room 3

Chair: [Rached Tourki; Faculté des Sciences de Monastir, Tunisia](#)
[Tay-Jyi Lin; National Chiao Tung Univ, Taiwan](#)

Robust Color Image Watermarking Based on Singular Value Decomposition and Dual Tree Complex Wavelet Transform

Samira Mabtoul, *U. Mohamed V*; El Hassan Ibn Elhaj, *Institut National des Postes et Telecommunications*; Driss Aboutajdine, *LRIT-GSCM, U. Mohamed V Rabat*

A New Blind Image Watermarking Technique for Dual Watermarks Using Low-Frequency Band DCT Coefficients

Ahmed Al-Gindy, Ayman Tawfik, *Ajman U. of Science & Technology*; Hussain Al-Ahmad, *Etisalat U. College*; Rami Qahwaji, *U. of Bradford*

An Improved SDA Approach with DFB PREPROCESSING for Face Recognition

Walid Boukabou, Ahmed Bouridane, *Queens U., Belfast*; Camel Tanougast, *Nancy U. - U. Henri Poincaré*

Tracking Objects in Videos with Texture Features

John Klein, Christele Lecomte, Pierre Miche, *LITIS*

A Novel Burst Correction Coding for the Images

Abolfazl Lakdashti, *Rouzbahan Institute of Higher Education*; Hedayat Kialashaki, *U. of Applied Science and Technology*; Mohammad-T Manzuri-Shalmani, *Sharif U. of Technology*; Hossein Ajourloo, *Iran Telecommunication Research Center*

B2L-E Microwave Circuits and Structures

Place: Room 4

Chair: [Marko Krcmar; Berlin U. of Technology, Germany](#)
[Balwant Godara; ISEP, France](#)

A Mixed Ladder-Lattice Bulk Acoustic Wave Duplexer for W-CDMA Handsets

Alexandre Shirakawa, Jean-Baptiste David, Pierre Vincent, *CEA LETI - MINATEC*; Moustapha El Hassan, Eric Kerhervé, *Bordeaux U.*; Andreia Cathelin, *STMicroelectronics*

Theoretical and Experimental Investigations of Multiple Resonant Frequencies in Single Negative Metamaterials

Soumia Massaoudi, Isabelle Huynen, *U. Catholique de Louvain*

Antenna Design Method for RFID UHF Tags

Plamen Iliev, *U. de Nice-Sophia Antipolis and ASK, Sophia Antipolis*; Philippe Le Thuc, Cyril Luxey, Robert Staraj, *U. de Nice-Sophia Antipolis*

A 2 Pole Micromachined Bandpass Filter at 150 GHz

Raghida Hajj, Matthieu Chatras, Pierre Blondy, *XLIM Research Institute*; J.C. Orhac, *Astrium EADS*; C. Goldstein, J. Puech, *CNES*

B2L-F TUTORIAL 7: EMBEDDED TUTORIAL

Place: Room 5

Chair: [Ali Ahaitouf; Fès, Morocco](#)

Simulation of electromagnetic radiation produced by integrated circuits

Jean-Yves Oberlé, *Texas Instruments, France*

B3P-G Communications, Sensors and RF systems

Place: Poster Area 1

Chair: A. Kherras; EMI, Morocco

VHDL-AMS Modeling of an UWB Radio Link Including Antennas

Rami Khouri, Yvan Duroc, Vincent Beroulle, Smail Tedjini, *INP Grenoble - LCIS*; Osman Francisco Oliveira Gomes, *Campina Grande - PB*

Efficient Reference Signal Cancellation in a Passive Radar

Pawel Biernacki, *U. of Technology Wroclaw*

30GHz Amplifiers with 0.25um SiGe BiCMOS

Jorge Torres, *Instituto Militar dos Pupilos do Exército*; João Caldinhas Vaz, João Costa-Freire, *Instituto Superior Técnico*

Theoretical and Simulation of Crosstalk Between Two Strip Lines Using Multiconductor Transmission Line

Said Ghnimi, Adnen Rajhi, Ali Gharsallah, *Faculté des Sciences de Tunis*

Reduction of Power Consumption in a Viterbi Decoder for OFDM-WLAN

Fabian Angarita Preciado, Maria Jose Canet Subiela, Trinidad Sansaloni Balaguer, Vicenç Almenar Terre, Javier Valls Coquillat, *Universidad Politécnica de Valencia*

SecurID Authenticator: on the Hardware Implementation Efficiency

Nicolas Sklavos, *U. of Patras*; Costas Eftstathiou, *TEI of Athens*

Efficient and Effective VLSI Architecture for a Wavelet-Based Broadband Sonar Signal Detection System

Sheng Cheng, Chien-Hsun Tseng, Marina Cole, *U. of Warwick*

A Wideband CMOS LNA Integrated with Balun and Linear Digital Gain Control

Fernando Azevedo, Fernando Fortes, *Instituto Superior de Engenharia de Lisboa*; João Vaz, *Instituto Superior Técnico / Instituto de Telecoms*; M. João Rosario, *Instituto Superior Técnico*

A Real-Time Admission Control and Planning of OLS Networks

Yassine Khelifi, Noureddine Boudriga, *U. of Carthage*; Mohammad Obaidat, *Monmouth U.*

Design and Implementation of a 1-V Low Flicker Noise Direct Conversion Mixer at 5.5 GHz Using a 90nm CMOS RF Technology

Simitsakis Paschalis, Kitonaki Eleni-Sotiria, Bazigos Antonios, Papananos Yannis, *National Technical U. of Athens*

Characterization Test Plan for a PCB to Die Transition in a fcCBGA Application

Joseph Romen Cubillo, Jean Gaubert, Sylvain Bourdel, Hervé Barthélemy, *L2MP*

Advanced Model and RF-CMOS Design of the Boot-Strapped Inductor

Domenico Zito, Alessandro Fonte, Bruno Neri, *U. of Pisa*

Performance Analysis of Single Code Spread ALOHA Systems

Ali Hellany, Hassan Achi, *U. of Western Sydney*

Design of the Microstrip Antennas $\lambda/8$ for Wireless Communications "by TLM Model"

Latif Adnane, Rachid Hilal, Abdellah Ait Ouahman, *U. Cadi Ayyad*

B4L-A SPECIAL SESSION: Design of Wireless Sensor Networks - The ANGEL Project Approach

Place: Auditorium

Chair: Pierangelo Garino, *Telecom Italia S.p.A., Italy*

Angel System & Platform Architecture

Jacques Bruynen, *NXP Semiconductors*; Marco Nalin, *Fondazione Centro San Raffaele del Monte Tabor*; Pierangelo Garino, *Telecom Italia*; Marco Decandia, *SESA*

Co-Simulation Framework for the Angel Platform

Andrea Bragagnini, *Telecom Italia*; Franco Fummi, *Universita di Verona*; Axel Huebner, *Philips Research Europe*; Giovanni Perbellini, Davide Quaglia, *U. of Verona*

The ANGEL WSN Architecture

Andreas Willig, Jan-Hinrich Hauer, Niels Karowski, *Technical U. of Berlin*; Heribert Baldus, Axel Huebner, *Philips Research Europe*

Gateway and Middleware Design: Trusted WSN-TLC Network Communication and Enhanced WSN Management

Elisa Alessio, Andrea Bragagnini, *Telecom Italia*; Giovanni Perbellini, Davide Quaglia, *U. of Verona*

Trustworthiness: Safety, Security and Privacy Issues

Janusz Górski, Grzegorz Golaszewski, Jakub Miler, Maciej Piechówka, *Gdansk U. of Technology*; Heribert Baldus, *Philips Research Europe*

B4L-B Phase Shifters and Auto-Tuning

Place: Room 1

Chair: Gilson Wirth; *U Federal do Rio Grande do Sul, Brazil*
Abdollah Khoei; *Urmia U., Iran*

An Efficient Design Procedure for High-Speed Low-Power Dual-Modulus CMOS Prescalers
Ranganathan Desikachari, *Cambridge Silicon Radio Ltd.*; Mark Steeds, Jeffrey Huard, *National Semiconductor Corp.*; Un-Ku Moon, *Oregon State U.*

A Novel CMOS Wideband Auto-Tuning Phase Shifter Circuit
Saad Al-Shahrani, *King Fahd U. of Petroleum and Minerals*

An Open Loop Phase Shifter and Frequency Synthesizer
Sarang Kazemi Nia, Khayrollah Hadidi, Abdollah Khoei, *Urmia U.*

OTA Based Frequency Tuning System

Chrisostomos Kasimis, George Souliotis, Costas Psychalinos, *U. of Patras*

B4L-C Pipelined ADCs

Place: Room 2

Chair: Vincent Frick; *Institut d'Electronique du Solide et des Systèmes, France*

Power Optimization of Pipelined ADCs with High-Order Digital Gain Calibration

Mohammad Taherzadeh-Sani, Anas Hamoui, *McGill U.*

Optimization of Pipelined ADC Architecture for Monolithic Active Pixel Sensors

Mokrane Dahoumane, Daniel Dzahini, Joel Bouvier, Eric Lagorio, Olivier Rossetto, Jean-Yves Hostachy, *Laboratoire de Physique Subatomique et de Cosmologie*; Hamid Ghazlane, *CNESTAN*; D. Dallet, *IXL*

A Pipelined 12-Bit Analog-to-Digital Converter with Continuous on-Chip Digital Correction

Ndubuisi Ekekwe, *Johns Hopkins U.*; Chinyeaka Ekenedu, *Blekinge Institute of Technology, Sweden*

A 10-Bit, 1.8-Gs/S Time-Interleaved Pipeline ADC

Väinö Hakkarainen, *Helsinki U. of Technology*; Arto Rantala, *VTT Information Technology*; Mikko Aho, Jaana Riikonen, *Helsinki U. of Technology*; David Gomes-Martin, Markku Aberg, *VTT Information Technology*; Kari Halonen, *Helsinki U. of Technology*

A Capacitor Mismatch- and Nonlinearity-Insensitive 1.5-Bit Residue Stage for Pipelined ADCs

Mehdi Saber, Reza Lotfi, *Ferdowsi U. of Mashhad*

B4L-D Digital Signal Processing Applications

Place: Room 3

Chair: Hussain Al-Ahmad; *Etisalat U. College, UAE*
Radu Matei; *Technical Univ 'Gh.Asachi', Romania*

Perfectly Balanced Binary Sequences with Optimal Autocorrelation

Syed Faisal Shah, Ahmed Tewfik, *U. of Minnesota*

Turbo Code Based Detection for Audio Watermarking: the Generalized Gaussian Noise Channel Model

Taoufik Majoul, Fathi Raouafi, Meriem Jaidane, *U2S, Ecole Nationale d'Ingénieurs de Tunis*

Blind Separation of Cyclo-Stationary Signals Using Generalized Eigenvalue Approach

Tarik Aoufi, *Faculté des Sciences, Battouta*; M'Hamed Bakrim, *Faculté des Sciences et Techniques, Marrakech*; Driss Aboutajdine, *LRIT-GSCM, U. Mohamed V Rabat*

Discrete Frequency-Coding Waveform Design

Sohanpal Singh, *MGIT*; Kakarla Subbarao, *U. College of Engg. Osmania U.*

B4L-E SoC Methodology and Applications **Place: Room 4**

Chair: [Peter Nilsson; Lund Univ, Sweden](#)

A Dynamic Clock Switch for Automotive System on Chip
Luca Bacciarelli, *Universita' di Pisa*; Luca Mostardini, Luca Fanucci, *U. of Pisa*; Alessandro Iannuzzi, Lorenzo Bertini, Marco De Marinis, *SensorDynamics AG*

A Design Methodology for Power Electronics Digital Control Based on an FPGA in the Loop Prototyping
Shahram Karimi, Philippe Poure, Yves Berviller, Shahrokh Saadate, *Nancy U. - U. Henri Poincaré*

Accurate Analysis of Switching Patterns in High Speed on-Chip Global Interconnects
Abinash Roy, Sharada Jha, Masud Chowdhury, *U. of Illinois at Chicago*

A Generic IP Core of the Identical Forward and Inverse 12/36-Point MDCT Architecture and an Architectural Model Simulation Toolbox
Peter Malik, *Slovak Academy of Sciences*

Bit-Level Optimization of Shift-and-Add Based FIR Filters
Kenny Johansson, Oscar Gustafsson, Lars Wanhammar, *Linköping U.*

B4L-F Algorithms and Techniques for Architecture Exploration **Place: Room 5**

Chair: [Menouer Boubekeur; U. College Cork, Ireland](#)
[Mehdi Kamal; Sharif Univ of Technology, Iran](#)

Timing-Driven Steiner Tree Construction with Wire Sizing, Buffer Insertion and Obstacle Avoidance
Jin-Tai Yan, Shi-Qin Huang, Zhi-Wei Chen, *Chung-Hua U.*

Hardware Architectures for the Generalized Finite Automata Algorithm
Abdel Ejnoui, *U. of South Florida Lakeland*; Paul Bao, *U. of South Florida Lakeland, Information Technology Dept.*

Order Independent Switching Operations in Radially Operated Networks
Pedro Carvalho, Alena Kostalova, Luís Ferreira, *Instituto Superior Tecnico, UTL*

No-Handshake Asynchronous Survivor Memory Unit for a Viterbi Decoder
Wei Shao, Linda Brackenbury, *U. of Manchester*

Dual Mode K-Best MIMO Detector Architecture and VLSI Implementation
Ramin Shariat-Yazdi, Tadeusz Kwasniewski, *Carleton U.*

Thursday, December 13, 2007, 14:00 - 14:45

B5L-A Keynote: Didier Lattard **Place: Auditorium**

Chair: [Eric Kerhervé; Bordeaux Univ, France](#)

Trends in Complex SoC Design: From Technology Variability to Multiprocessor Architectures
Didier Lattard, *CEA*

Thursday, December 13, 2007, 14:45 - 15:30

B6L-A Keynote: Kiyoo Itoh

Place: Auditorium

Chair: Yvon Savaria; *École Polytechnique, Canada*

Low-Voltage Limitations and Challenges of Memory-Rich Nano-Scale CMOS LSIs
Kiyoo Itoh, *Hitachi*; Riichiro Takemura, *Hitachi CRL*

Thursday, December 13, 2007, 15:35 - 17:05

B7L-A SPECIAL SESSION: Device Modeling and Simulation

Place: Auditorium

Chair: Andrei Vladimirescu; *U. of California, Berkeley, USA*

Optimal Design Methodology for High-Order Continuous-Time Wideband Delta-Sigma Converters

Yi Ke, Soheil Radiom, Hamidreza Rezaee, Guy Vandenbosch, *Katholieke Universiteit Leuven*; Jan Craninckx, *IMEC*; Georges Gielen, *Katholieke Universiteit Leuven*

System-Level Design for Nano-Electronics

David Atienza, *Ecole Polytechnique Federale de Lausanne*; Shashi Kanth Bobba, *LSI/EPFL*; Massimo Poli, *U. of Siena*; Giovanni De Micheli, *LSI/EPFL*; Luca Benini, *DEIS/Bologna U.*

Sizing Low-Voltage CMOS Analog Circuits

Paul L. Jespers, *U. Catholique de Louvain*

Advanced Statistical Methodology for 6T-SRAM Design

Cédric Maufmont, Richard Ferrant, *STMicroelectronics*

B7L-B Regulators and References

Place: Room 1

Chair: Savas Kaya; *Ohio Univ, USA*
Hassan Mahmoudi; *EMI, Morocco*

Rectangular Wave Delta Modulation Buck Regulator

Jitkasame Ngarmnil, Kriangkrai Sooksood, *Mahanakorn U. of Technology*

Structural Design of a CMOS Full Low Dropout Voltage Regulator

Igor Filanovsky, *U. of Alberta*; Mahub Reja, *Scanimetrix, Inc.*; Vadim Ivanov, *TI*.

High-Accuracy Low-Dropout Voltage Regulator Based on Slow-Rolloff Frequency Compensation

Liangguo Shen, *Peking U.*; Zu-Shu Yan, *Beijing Microelectronics Technology Institute*; Xing Zhang, *Peking U.*; Yuan-Fu Zhao, *Beijing Microelectronics Technology Institute*

A Novel Precise Step-Shaped Soft-Start Technique for Integrated DC-DC Converter

Chun-Yu Hsieh, Yung-Chun Chuang, Ke-Horng Chen, *National Chiao Tung U.*

Impact of Noise on Trim Circuits for Bandgap Voltage References

Dalton Colombo, Gilson Wirth, *U. Federal do Rio Grande do Sul*; Sergio Bampi, *Federal U. of Rio Grande do Sul*; Christian Fayomi, *U. du Québec à Montreal*

B7L-C Memory and other Issues in Communications

Place: Room 2

Chair: Michael De Nil; *IMEC-NL and Eindhoven Univ of Technology, Netherlands*
Mustapha Alami; *INPT, Morocco*

Frame Based Memory Access Interpolation for a Digital Communication Modulator

Ruimin Huang, Markus Becker, *U. of Freiburg - IMTEK*; Niklas Lotze, *U. of Freiburg*; Yiannos Manoli, *U. of Freiburg - IMTEK*

High-Speed, Low Cost Parallel Memory-Based FFT Processors for OFDM Applications

Chin-Long Wey, Shin-Yo Lin, Wei-Chien Tang, Muh-Tien Shiue, *National Central U.*

A Low-Complexity High-Performance Modulation Code for Holographic Data Storage

Chi-Yun Chen, Tzi-Dar Chiueh, *National Taiwan U.*

A QoS-Oriented Scheme for a Real Time Admission Control in OBS Networks

Amor Lazzez, Nouredine Boudriga, *U. of Carthage*

Roundoff Noise Analysis for FSK Signals in White Noise Represented as Signed Power-of-Two Numbers

Ya Jun Yu, Yong Ching Lim, *Nanyang Technological U.*

B7L-D Digital Filter Design II

Place: Room 3

Chair: Gordana Jovanovic Dolecek; *Institute INAOE, Mexico*
Fernando Pescador Del Oso; *Univ Politécnic de Madrid, Spain*

A New Method for Initializing Real Second Order IIR Notch Filters

Jeedella Jeedella, Hussain Al Ahmad, Mohammed Al Mualla, *Etisalat U. College*; Jim Noras, *U. of Bradford*

Low Power Non-Recursive Decimation Filters

Chi Zhang, Erwin Ofner, *Carinthia U. of Applied Sciences*

A Digital Multistandard Reconfigurable FIR Filter for Wireless Applications

Fabio Gallazzi, Guido Torelli, Piero Malcovati, Vincenzo Ferragina, *U. of Pavia*

Design and Implementation of a Decimation Filter for High Performance Audio Applications

Khalid Abed, *Jackson State U.*; Shailesh Nerurkar, Stephen Colaco, *ASIC Advantage, Inc.*

Designing FIR Filter with Variable Stopbands

Naoyuki Aikawa, *Nihon U.*; Yukio Mori, *Salesian Polytechnic*

B7L-E RF CMOS

Place: Room 4

Chair: Masud Chowdhury; *Univ of Illinois at Chicago, USA*
Chiennan Kuo; *National Chiao Tung Univ, Taiwan*

A Broadband Folded Gilbert-Cell CMOS Mixer

Marko Krcmar, *Berlin U. of Technology*; Solon Spiegel, *Rio System*; Frank Ellinger, *Dresden U. of Technology*; Georg Boeck, *Berlin U. of Technology*

CMOS Power Amplifier with ESD Protection Design Merged in Matching Network

Yu-Da Shiu, Bo-Shih Huang, *Indust. Techno Research Inst.*; Ming-Dou Ker, *Nat'l Chiao-Tung U.*

An Integrated 60-GHz Front-End Receiver with a Frequency Tripler Using 0.13- μ m CMOS Technology

Po-Hung Chen, Min-Chiao Chen, Chung-Yu Wu, *National Chiao-Tung U.*

Radio Frequency Polyphase Filter Design in 0.13- μ m CMOS for Wireless Communications

Fayrouz Haddad, Rachid Bouchakour, Wenceslas Rahajandraibe, Lakhdar Zaid, *U. of Provence*; Oussama Frioui, *L2MP*

Integrated Tunable RF Filter for TV Reception [42MHz..870MHz]

Mohamed Bouhamame, Sébastien Amiot, Olivier Crand, Luca Lo Coco, Jean Marc Paris, Markus Kristen, Jean Robert Tourret, Xavier Pruvost, *NXP Semiconducteurs*; Serge Toutain; *Institut de Recherche en Electronique et Electrotechnique de Nantes Atlantique*

B7L-F Circuit Level Optimizations

Place: Room 5

Chair: Luis Mendes; *Instituto Politecnico de Leiria, Portugal*

Total Ionizing Dose Effects in Switched-Capacitor Filters using Oscillation-Based Test

John M. Espinosa, Jaime Velasco, *U. del Valle*; Gloria Huertas, Jose L. Huertas, *IMSE-CNM*

Buffer Insertion and Sizing in Clock Distribution Networks with Gradual Transition Time Relaxation for Reduced Power Consumption

Sherif Tawfik, Volkan Kursun, *U. of Wisconsin, Madison*

Routability-Driven Track Routing for Coupling Capacitance Reduction

Jin-Tai Yan, Zhi-Wei Chen, Kuen-Ming Lin, *Chung-Hua U.*

Lyapunov Stability of Hybrid System Limit Cycle Application to the Compass Gait Biped

Oumnia Licer, *Faculté des Sciences et Techniques, Fes*; Nouredine El Alami, *EMI Maroc*; Mostafa Mrabti, *Faculté des Sciences et Techniques, Fes*

Chair: A. Kherras; EMI, Morocco

Efficiency of Components' Region-Constrained Placement to Reduce FPGA's Dynamic Power Consumption

Sayed Ebrahim Esmaeili, Nabil Khachab, *Kuwait U.*

Architectural and Control Contributions for PV Grid-Connected Systems Applying Dual-Stage Inverters

Marcio M. Casaro, *Fed U. of Technology - Paraná*; Denizar C. Martins, *Fed U. of Santa Catarina*

A Comparative Implementation of PCA Face Recognition Algorithm

Nicolas Morizet, Frédéric Amiel, Insaf Dris Hamed, Thomas Ea, *Inst. Sup. d'Electronique de Paris*

Algebraic PWM Strategy of a Multilevel NPC Voltage Source Inverter

D Boufassa, Farid Bouchafaa, *U. of Science and Technology Houari Boumediene*; El Madjid Berkouk, *École Nationale Polytechnique*; M.S. Boucherit, *Polytechnic National School Algiers*

High-Gain Observer Compensator for Rotor Resistance Variation on Induction Motor RFOC

Ahmed Abbou, *Ecole Mohammadia d'Ingénieurs*; Hassan Mahmoudi, *Ecole Mohammadia d'Ingénieurs*; Abdelhadi Elbacha, *Faculté des Sciences et Techniques, Marrakech*

Improving Power Efficiency and Reliability in RF Tire Pressure Monitoring Modules

Fabrizio Iacopetti, Sergio Saponara, Luca Fanucci, *U. of Pisa*

CAD Methodology for Analog Static CMOS Design Automation

François Rudolff, Edith Kussener, *L2MP - ISEN, Toulon*; Gaëtan Bracmard, *ATMEL Rousset*

Reducing Power Consumption in NoC Design with No Effect on Performance and Reliability

Ahmad Patooghy, M. Fazeli, S.G. Miremadi, *Sharif U. of Technology*

A New ANFIS Based Learning Algorithm for CMOS Neuro-Fuzzy Controllers

Alireza Peymanfar, Abdoloh Khoei, Khayrollah Hadidi, *Urmia U.*

The Effect of Stator Resistance Variation on DTFC of Induction Motor and its Compensation

Ahmed Abbou, *Ecole Mohammadia d'Ingénieurs*; Hassan Mahmoudi, *Ecole Mohammadia d'Ingénieurs*; Abdelhadi Elbacha, *Faculté des Sciences et Techniques, Marrakech*

The Use of Simulated Annealing with Fuzzy Objective Function to Optimal Frequency Selection for Analog Circuit Diagnosis

Damian Grzechca, Tomasz Golonek, Jerzy Rutkowski, *Silesian U. of Technology*

Application of Diversity Controlled Genetic Algorithms to the Design and Optimization of OTA-C IF Filters

Yifan Wu, Behrouz Nowrouzian, *U. of Alberta*

Performance Analysis of Embedded Multiprocessor Industrial Applications: Methodology and Tools

Ismail Assayad, *Verimag*; Sergio Yovine, *CNRS/VERIMAG*

FPGA-Based Low-Cost System for Automatic Tests on Digital Circuits

Luca Mostardini, Luca Bacciarelli, Luca Fanucci, *U. of Pisa*; Lorenzo Bertini, Marco Tonarelli, Adolfo Giambastiani, Marco De Marinis, *SensorDynamics AG*

Thursday, December 13, 2007, 17:30 - 19:00

B9L-A SPECIAL SESSION: Low Power Design Techniques

Place: Auditorium

Chair: Christian Piquet; *CSEM, Switzerland*

Low Power Design in Deep Submicron 65 & 45 nm Technologies
Christian Piquet, *CSEM*

Logic Design Techniques for 65 to 45nm and Below for Reducing Total Energy and Solving Technology Variations Problems
Domenik Helms, *Offis*; Wolfgang Nebel, *U. of Oldenburg*

How to Use High-Level Models to Optimize Power and Energy in Processors in 45 & 65 nm Technologies
Nathalie Julien, *U. de Bretagne-Sud*

Solutions for Logic and Processor Core Design at the 45nm Technology Node & and Below
Philippe Royannez, Hugh Mair, Michael Clinton, Uming Ko, *Texas Instruments, France*

Power-Limited Design
Borivoje Nikolic, *U. of California, Berkeley*

B9L-B UWB Circuits and Systems

Place: Room 1

Chair: Özhan Koca; *Univ of Erlangen-Nuremberg, Germany*

An Offset Compensated Baseband Circuit for Automotive Radar Ultra-Wideband Applications

Vittorio Salvatore Giannello, Egidio Ragonese, Giuseppe Palmisano, *U. of Catania*; Angelo Scuderi, *STMicroelectronics*

Application of the Superregenerative Principle to UWB Pulse Generation and Reception
F. Xavier Moncunill-Geniz, *U. Politècnica de Catalunya*; Pere Palà-Schönwälder, *U. Politècnica de Catalunya-Technical U. of Catalonia*; Francisco Del Águila-López, Rosa Giralt-Mas, *U. Politècnica de Catalunya*

Ultra Wide Band Band Pass Filter Embedding a MLF Low Cost Package with Wire Bound Attach Process

Joseph Romen Cubillo, Jean Gaubert, Sylvain Bourdel, Herve Barthélemy, Marc Battista, Matthieu Egels, *L2MP*

B9L-C Mixed-Signal Circuits

Place: Room 2

Chair: Philippe Benabes; *SUPELEC, France*

ECG Signal Artifacts Suppression System Based on an MRI Environment Dedicated CMOS Magnetic Field Monitor and FPGA Implementation

Vincent Frick, Hervé Berviller, Joris Pascal, Philippe Bougeot, Jean-Philippe Blondé, *Institut d'Electronique du Solide et des Systèmes*; Julien Oster, Jacques Felblinger, *Imagerie Adaptative Diagnostique et Interventionnelle*

Built-in Filtering for Out-of-Channel Interferers in Continuous-Time Quadrature Bandpass Delta Sigma Modulators

Nejmeddine Joudia, Chiheb Rebai, Adel Ghazel, *Ecole Supérieure des Communications de Tunis*; Dominique Dallet, *U. of Bordeaux 1*

Design of a New CMOS Controllable Mixed-Signal Current Mode Fuzzy Logic Controller (FLC) Chip

Ghader Yosefi, Abdollah Khoei, Khayrollah Hadidi, *Urmia U.*

Phase Data Converter Design for IEEE 802.15.4-Based Wireless Receiver

Souha Masmoudi, *Cité Technologique des Communications*; Adel Ghazel, *Ecole Supérieure des Communications de Tunis*; Patrick Loumeau, *Telecom Paris*

B9L-D Digital Filter Design III

Place: Room 3

Chair: Marina Dana Topa; *Technical Univ of Cluj-Napoca, Romania*
Imad El Mourabit; *ENSAT Tanger, Morocco*

Directional Zero-Phase 2D IIR Filter Design Using Chebyshev- Padé Approximation

Radu Matei, *Technical U. 'Gh.Asachi'*

Fractional-Order Digital Phase-Locked Loop

Reyad El-Khazali, *Etisalat U. College*

On a MULTIPLIERLESS FIR Decimation Filter Design

Gordana Jovanovic Dolecek, Naina Rao Nagrale, *Institute INAOE*

Reconfigurable DSP Architectures for SDR Applications

Najam-Ul-Islam Muhammad, *Institute Eurecom*; Karim Khalfallah, Raymond Knopp, *Institute Eurecom*; Renaud Pacalet, *ENST- Lab SoC*

B9L-E Reconfigurable and FPGA Systems

Place: Room 4

Chair: Lilian Bossuet; *Univ of Bordeaux 1, France*
Makoto Ikeda; *U. of Tokyo, Japan*

A VLSI Architecture for a Run-Time Multi-Precision Reconfigurable Booth Multiplier

Zhou Shun, *Hong Kong U. of Science and Technology*; Oliver Pfaender, Hans-Jörg Pfeleiderer, *U. of Ulm*; Amine Bermak, *Hong Kong U. of Science and Technology*

Cluster-Based Hybrid Reconfigurable Architecture for Auto-Adaptive SoC

Xun Zhang, Hassan Rabah, Serge Weber, *Nancy U. - U. Henri Poincaré*

A Methodology to Evaluate the Energy Efficiency of Application Specific Processors

Nicolas Beucher, Normand Bélanger, Yvon Savaria, Guy Bois, *École Polytechnique de Montréal*

Low Complexity Synchronization and Frequency Equalization for OFDM Systems

F. Javier Lopez-Martinez, Eduardo Martos-Naya, J. Tomas Entrambasaguas, *Universidad de Malaga*; Maria Garcia-Abril, *GCM Communications Technology*

B9L-F Networks and Multiprocessors on Chip

Place: Room 5

Chair: Gabriela Nicolescu; *Ecole Polytechnique de Montreal, Canada*
Abdel Ejnoui; *Univ of South Florida Lakeland, USA*

An Isometric on-Chip Multiprocessor Architecture

Etienne Ogoubi, Abdelhakim Hafid, *U. de Montréal*; Marcel Turcotte, *U. of Ottawa*

An FPGA Implementation of a Scalable Network-on-Chip Based on the Token Ring Concept

Karim Hadjiat, Francis St-Pierre, Guy Bois, Yvon Savaria, *École Polytechnique de Montréal*; Michel Langevin, Pierre Paulin, *STMicroelectronics*

MIC@R : a Generic Low Latency Router for on-Chip Networks

Rafik Ben Tekaya, *UBS U. and Faculty of Sciences at Monastir*; Adel Baganne, *UBS U.*; Rached Tourki, *Faculté des Sciences de Monastir*

SOPC-Based Architecture for Discrete Particle Swarm Optimization

Amin Farmahini-Farahani, Sied Mehdi Fakhraie, Saeed Safari, *U. of Tehran*

Reducing the Power Consumption in Networks-on-Chip Through Data Coding Schemes

José Carlos Palma, *UFRGS*; Leandro Indrusiak, *TU-Darmstadt*; Fernando Moraes, *PPGCC - FACIN - PUCRS*; Ricardo Reis, *U. Federal do Rio Grande do Sul*; Manfred Glesner, *TU-Darmstadt*

Friday, December 14, 2007, 08:30 - 09:15

C1L-A Invited Talk: Takayuki Kawahara

Place: Auditorium

Chair: Mounir Boukadoum; *UQAM, Canada*

SPRAM (SPin-transfer torque RAM) Design and its Impact on Digital Systems
Takayuki Kawahara, R. Takemura, H. Takahashi, *Hitachi Ltd.*; H. Ohno, *Tohoku U.*

Friday, December 14, 2007, 09:20 - 10:50

C2L-A Power Management

Place: Auditorium

Chair: Amine Bermak; *Hong Kong Univ of Science and Technology, Hong Kong*
Jamal El Abbadi; *EMI, Morocco*

Power Profile Evaluation of Battery-Powered Mobile Applications
Marius Marcu, Dacian Tudor, *Politehnica U. of Timisoara*; Horatiu Moldovan, *Lasting System SRL*;
Mihai Micea, *Politehnica U. of Timisoara*

Feedback Driven Adaptive Power Management for Minimum Power Operation of Wireless Receivers
Shreyas Sen, Rajarajan Senguttuvan, Abhijit Chatterjee, *Georgia Institute of Technology*

Architecture for a Low Power Image Sensor with Motion Detection Based ROI
Arnaud Verdant, Patrick Villard, *CEA LETI - MINATEC*; Antoine Dupret, Hervé Mathias, *U. Paris Sud*

Power-Efficient and Low Latency Implementation of Programmable FIR Filters Using Carry-Save Arithmetic
Dimitris Bekiaris, Isidoros Sideris, George Economakos, Kiamal Pekmestzi, *National Technical U. of Athens*

C2L-B Analog and RF Modeling

Place: Room 1

Chair: Yngvar Berg; *Univ of Oslo, Norway*
M. El Adnani; *ENSA Marrakech, Morocco*

Pspice Behavior and Thermal Modeling of the Pin Diode: a Circuit Approach
Elmostafa Elwarraki, *U. Cadi Ayyad*; Abderrafia Sabir, *Hassan II U.*

Designing SRCOs by Symbolic-Behavioral-Modeling of Unity-Gain Cells
Esteban Tlelo-Cuautle, *Institute INAOE*; Carlos Sánchez-López, *Universidad Autónoma de Tamaulipas, Mexico*; Mourad Fakhfakh, Mourad Loulou, *National Engineering School of Sfax*

Analysis of Nonlinear Switched Circuits with Different State Variables in Each Topology
Francisco Del-Águila, *U. Politècnica de Catalunya*; Pere Palà-Schönwälder, *U. Politècnica de Catalunya-Technical U. of Catalonia*; Jordi Bonet, F. Xavier Moncunill, Rosa Giral, *U. Politècnica de Catalunya*

C2L-C Radio Techniques

Place: Room 2

Chair: Hossam Fahmy; *Ain Shams Univ, Egypt*

An IF Digital Down-Converter for Software Radio DVB-S2 Receivers

Panayiotis Savvopoulos, Theodore Antonakopoulos, *U. of Patras*

Evaluation of the Performances of ANN and SVM Techniques Used in Water Quality Classification

Mohamed Bouamar, Mohamed Ladjal, *Laboratoire d'Analyse des Signaux et Systèmes*

Radio-Based Cooperation Scheme for DDoS Detection

Amel Makhoulf, *U. of 7th of November, Carthage*; Nouredine Boudriga, *U. of Carthage*; Mohammad Obaidat, *Monmouth U.*

A Reconfigurable IR-UWB Radio Interface, with Directional Antennas and Localization Capability, for Wireless Sensor Networks

Aubin Lecointre, Daniela Dragomirescu, Pascal Berthou, Robert Plana, *U. of Toulouse*

Multi-Carrier CDMA-Interconnect for Inter- and Intra-ULSI Communications

Md Sajjad Rahaman, Masud Chowdhury, *U. of Illinois at Chicago*

C2L-D Sensor Design

Place: Room 3

Chair: Kyriaki Minoglou; *TEI of Pireaus, Greece*
Jamal El Abbadi; *EMI, Morocco*

A High Dynamic Range Time-Based Edge Detection Algorithm for a Vision Sensor

Massari Nicola, Arsalan Jawed Syed, Massimo Gottardi, *Fondazione Bruno Kessler-IRST*

CMOS X-Ray Image Sensor Array

Jose Silva, Senentxu Lanceros-Mendez, Graca Minas, Jose Rocha, *U. of Minho*

A Two-Stage Capacitive-Feedback Differencing Amplifier for Temporal Contrast IR Sensors

Christoph Posch, Daniel Matolin, Rainer Wohlgenannt, *Austrian Research Centers*

POSFET Based Tactile Sensor Arrays

Ravinder Dahiya, *Italian Institute of Technology & U. of Genova*; Maurizio Valle, *U. of Genova*; Giorgio Metta, *Italian Institute of Technology & U. of Genova*; Leandro Lorenzelli, *Fondazione Bruno Kessler-IRST*

High-Speed Industrial Vision Applications Using an Embedded Smart Sensor System

Ahmed Nabil Belbachir, Karl Reisinger, Michael Hofstaetter, Peter Schön, *Austrian Research Centers*

C2L-E RF Oscillators

Place: Room 4

Chair: Marko Krcmar; *Berlin Univ of Technology, Germany*
 Domenico Zito; *Univ of Pisa, Italy*

Design Considerations and Device Selection in the Implementation of Low Phase Noise LC-VCOs

Owen Casha, Ivan Grech, Joseph Micallef, Edward Gatt, *U. of Malta*

Multiphase Signal Generation Using Capacitive Coupling of LC-VCOs

Malihe Zarre Dooghabadi, Sasan Naseh, *Ferdowsi U.*

A High-Performance Digitally Controlled LC Oscillator for Ku-Band Applications

Luis Mendes, *Instituto Politecnico de Leiria / Instituto de Telecomunicações*; Eduardo Pires, *U. de Trás-os-Montes e Alto Douro*; João Vaz, Maria Rosário, *Instituto Superior Técnico / Instituto de Telecomunicações*

A 2.4 GHz Very Low Phase Noise Fully Integrated Quadrature LC Oscillator

Oussama Frioui, *L2MP*; Lakhdar Zaid, Wenceslas Rahajandraibe, *U. of Provence*; Fayrouz Haddad, *L2MP*

Finding the Tuning Curve of a Complementary VCO

Antonio Buonomo, Alessandro Lo Schiavo, *Seconda Università di Napoli*

C2L-F Design For Test

Place: Room 5

Chair: Kunihiro Asada; *Univ of Tokyo, Japan*
 Abderahman Ayadi; *ENSA Safi, Morocco*

Improved Low Power Full Scan BIST

Umeh Parashar, *Dhirubhai Ambani Institute of Information and Communication Technology*

GABIST: a New Methodology to Find Near Optimal LFSR for BIST Structure

Mehdi Kamal, *Sharif U. of Technology*; Mehdi Salmani Jelodar, *U. of Tehran*; Shaahin Hessabi, *Sharif U. of Technology*

Multiple Parametric Circuit Analysis Tool for Detectability Estimation

Michael Dimopoulos, *Aristotle U. of Thessaloniki Greece*; Dimitris Papakostas, *Alexander Technological Educational Inst. of Thessaloniki, Greece*; Dimitrios Konstantinou, Alexios Spyronasios, Alkis Hatzopoulos, *Aristotle U. of Thessaloniki Greece*

A Heuristic Fault Dictionary Reduction Methodology

Andrzej Pulka, *Silesian U. of Technology*

An Embedded Test Circuit for RF Single Ended Low Noise Amplifiers

Lampros Dermentzoglou, Anastasios Karagounis, Aggeliki Arapoyanni, *U. of Athens*; Yiorgos Tsiatouhas, *U. of Ioannina*

Chair: Abdeslam Annaque; *EMI, Morocco*

A 0.65-0.9-1.2V Supplies 10MHz High Efficiency PWM CMOS Buck DC-DC Converter
Bilal Manai, Malik Bouguelaa, Xavier Rabeyrin, *ATMEL Rousset*

Low-Voltage BiCMOS Circuit Topologies for the Design of a 19GHz, 1.2V, 466mW, 4-Bit Accumulator in Silicon-Germanium
Ryan Bethel, David Kotecki, *U. of Maine*

A CMOS Transconductor with High Linear Range
Aimad El Mourabit, *ENSA de Tanger*; Mohamed Halim Sbaa, *STMicroelectronics*; Zine Abidine Alaoui-Ismaili, Fouad Lahjomri, *ENSA de Tanger*

Separation of convolutive Mixtures of Cyclo-Stationary Signals Using a Non-Unitary Block-Diagonalization Algorithm
H. Ghennioui, *Rabat and ISITV-Toulon*; S. Rhioui, N. Thirion-Moreau, Eric Moreau, *ISITV-Toulon*; A. Adib, *Institut Scientifique, Rabat*; D. Aboutajdine, *LRIT-GSCM, U. Mohamed V Rabat*

Symbolic Analysis Based on Graph Transformations
Zdenek Kolka, Martin Vlk, Dalibor Bielek, Viera Biolkova, *Brno U. of Technology*

The Triple Resonance Network with Sinusoidal Excitation
Antonio de Queiroz, *Federal U. of Rio de Janeiro*

Body-Driven Enhanced-Impedance Current Source: An Approach to the Implementation of Low-Voltage Current-Steering D/A Converters
Moslem Hokmabadi, *Integrated Systems Lab*; Alireza Zabihian, *Integrated Systems Lab, Ferdowsi U. of Mashhad, Iran*; Reza Lotfi, *Ferdowsi U. of Mashhad*

A Low Power Dual-Mode Sigma-Delta Modulator for gsm/wcdma Receivers
Inhee Lee, Youngcheol Chae, Gunhee Han, *Yonsei U.*

Blind Source Separation Based on Wavelet Signal Representation
Atman Jbari, *Faculté des Sciences, Rabat*; Abdellah Adib, *Institut Scientifique, Rabat*; Driss Aboutajdine, *LRIT-GSCM, U. Mohamed V Rabat*

Behavioral Modeling of a Programmable UWB/Bluetooth ADC
Martin Gustafsson, Ana Rusu, Mohammed Ismail, *Royal Institute of Technology*

A 100 MHz-1 GHz Adaptive Bandwidth PLL Using TDC Technique
Kuo-Hsing Cheng, *National Central U.*; Yu-Lung Lo, *Industrial Technology Research Institute*; Ching-Wen Lai, *National Central U.*; Wei-Bin Yang, *Industrial Technology Research Institute*

Design of a High Speed, Low Latency and Low Power Consumption DRAM Using Two-Transistor Cell Structure
Amin Chegeni, *U. of Urmia*; Khayrollah Hadidi, Abdollah Khoei, *Urmia U.*

How to Reduce Jitter in Fractional PLL
Z. Belfkih, Samir Bahbouhi, M. H. Sbaa, *STMicroelectronics*; A. El Mourabit, *ENSA Tanger*

Soft Power Up / Power Down on Digital to Analog Converter CMOS65
N. Barhouli, M. Halim Sbaa, H. Senhaji, *STMicroelectronics*; Aimad El Mourabit, *ENSA de Tanger*

Ripple Reduction in DTC Drives by Using a Three-Level NPC VSI
Iqbal Messaïf, *U. des Sc. et de la Techno. Houari Boumedienne*; El Madjid Berkouk, *École Nationale Polytechnique*; Nadia Saadia, *U. des Sc. et de la Techno. Houari Boumedienne*

C4L-A Embedded Systems

Place: Auditorium

Chair: Marius Marcu; *Politehnica Univ of Timisoara, Romania*
Dalila Chaidmi; *EMI, Morocco*

Low Power Implementation of Decimation Filters in Multistandard Radio Receiver Using Optimized Multiplication-Accumulation Unit

Nadia Khouja, Khaled Grati, *CIRTA'COM LABORATORY*; Adel Ghazel, *Ecole Supérieure des Communications de Tunis*

Performance Evaluation of FPGA-Embedded Web Servers

Sergio Cuenca, Angel Grediaga, Hector Llorens, Marco Albero, *U. of Alicante*

A New Control Method of Hybrid Active Filter Using a Feedforward Loop Tuned at 5th and 7th Harmonic Frequency

Mohamed Abdousalam, Philippe Poure, Shahrokh Saadate, *Nancy U. - U. Henri Poincaré*

Real-Time Flatness-Based Control of a DC Motor

Soufiene Bouallegue, Mounir Ayadi, *LARA Automatique*; Joseph Haggège, Mohamed Benrejeb, *Ecole Nationale d'Ingénieurs de Tunis*

Fuzzy Controller for Mobile Robots Using Evolvable Hardware

Ahmed Moustafa Zaki, Mohammed Elshafey, Gamal Ali, *Ain Shams U.*

C4L-B RF IC Design

Place: Room 1

Chair: Kuo-Hsing Cheng; *National Central Univ, Taiwan*
Belhaj Elgraini; *EMI, Morocco*

A Bias-Controlled Noise-Canceling CMOS Tuned Low Noise Amplifier for UWB Transceivers

Rezaul Hasan, Jie Li, *Massey U., New Zealand*

60 GHz SiGe LNA

Van-Hoang Do, *TES Electronic Solutions GmbH*; Viswanathan Subramanian, Georg Boeck, *Berlin U. of Technology*

A New on-Chip CMOS Active Balun Integrated with LNA

Fernando Azevedo, Fernando Fortes, *Instituto Superior de Engenharia de Lisboa*; M. João Rosario, *Instituto Superior Técnico*

The First All-Transistor Wideband (0 – 5GHz) Impedance Matching Network

Balwant Godara, *Institut Supérieur d'Electronique de Paris*; Alain Fabre, *Ecole Nationale Supérieure d'Electronique, d'Informatique et de Radiocommunications de Bordeaux*

A 0.35- μ m CMOS Mixer for 3.1-4.8 GHz UWB MB-OFDM Receivers

Farid Touati, *Sultan Qaboos U.*; Skander Douss, Mourad Loulou, *National Engineering School of Sfax*

C4L-C Data Converter Performance and I/O Circuits

Place: Room 2

Chair: Mohamad Sawan; *École Polytechnique, Canada*
Ounsa Roudies; *EMI, Morocco*

Signal Integrity Analysis of a High Precision D/A Converter

Olivier Valorge, *École Polytechnique de Montréal*; David Marche, Alain Lacourse, *LTRIM inc*;
Mohamad Sawan, Yvon Savaria, *École Polytechnique de Montréal*

Effect of Mismatch on Substrate Noise Coupling on Flash a/D Converters

Athanasios Stefanou, Georges Gielen, *Katholieke Universiteit Leuven*

A 10 Gsamples/S SiGe Track-and-Hold Amplifier with 8-bit Resolution

Paul Zammit, Ivan Grech, Joseph Micallef, Edward Gatt, *U. of Malta*

Analysis of Open Loop Track-and-Hold Circuits

Pieter Harpe, Hans Hegt, Arthur van Roermund, *Eindhoven U. of Technology*

Design of 2xVDD-Tolerant I/O Buffer with Considerations of Gate-Oxide Reliability and Hot-Carrier Degradation

Hui-Wen Tsai, *National Chung-Tung U.*; Ming-Dou Ker, *National Chiao-Tung U.*

C4L-D Image and Video Processing

Place: Room 3

Chair: Ya Jun Yu; *Nanyang Technological Univ, Singapore*
Mohamed Ouadou; *Faculté des sciences – Rabat, Morocco*

A Cross-Layer Approach for Dynamic Rate Allocation in H.264 Multi-User Video Streaming

Charles Yaacoub, Joumana Farah, Nancy Rachkidy, *Holy-Spirit U. of Kaslik*; Béatrice Pesquet-Popescu, *ENST- Paris*

A Real-Time H.264 MP Decoder Based on a DM642 DSP

Fernando Pescador Del Oso, Matias Javier Garrido, Cesar Sanz, Eduardo Juarez, Manuel Cesar Rodriguez, David Samper, *Universidad Politécnica de Madrid*

Robust Watermarking System Using Security Enhancement on Content Based Image Segmentation

Mohammed Suhail, *Bradford U.*; Mohammad Obaidat, *Monmouth U.*

Content-Adaptive Semi-Fragile Watermarking for Image Authentication

Mohammed Al-Mualla, *Etisalat U. College*

Subsampling Image Compression Using AI-Alaoui Backpropagation Algorithm

Rony Ferzli, *Arizona State U.*; Mohamad Adnan Al-Alaoui, *American U. of Beirut*

C4L-E IC Design

Place: Room 4

Chair: Konstantin Septinus; *Leibniz U of Hannover, Germany*
 Hassan Mahmoudi; *EMI, Morocco*

Efficient and Accurate Models of Output Transition Time in CMOS Logic
 Massimo Alioto, Massimo Poli, *U. of Siena*; Gaetano Palumbo, *U. of Catania*

All-Digital PLL Using Pulse-Based DCO
 Hong-Yi Huang, *National Taipei U.*; Jen-Chieh Liu, Kuo-Hsing Cheng, *National Central U.*

Analysis of Spatial Temperature Distribution in ICs
 Shirram Krishnamoorthy, Masud H. Chowdhury, *U. of Illinois at Chicago*

New MTCMOS Flip-Flops with Simple Control Circuitry and Low Leakage Data Retention Capability
 Zhiyu Liu, Volkan Kursun, *U. of Wisconsin, Madison*

Temperature-Adaptive Energy Reduction for Ultra-Low Power-Supply-Voltage Subthreshold Logic Circuits
 Ranjith Kumar, Volkan Kursun, *U. of Wisconsin, Madison*

C4L-F Modeling and Synthesis

Place: Room 5

Chair: Abdelhakim Khouas; *École Polytechnique, Canada*
 Dimitris Papakostas; *Alexander Techn Educ Inst of Thessaloniki, Greece*

Communication Structure Refinement Using Temporal Constraints Analysis
 A. Tsikhanovich, El Mostapha Aboulhamid, *U. de Montréal*; Guy Bois, *École Polytechnique de Montréal*

Performance Modeling and Analysis of Asynchronous Linear-Pipeline with Time Variable Delays
 Eslam Yahya, Marc Renaudin, *CIS-TIMA-INPG*

Logic and Physical Synthesis of Cell Arrays
 Cristina Meinhardt, Ricardo Reis, *U. Federal do Rio Grande do Sul*; Reginaldo Tavares, *U. Federal de Pelotas*

Process Variation Aware Comprehensive Layout Synthesis for Yield Enhancement in Nano-Meter CMOS
 Kenichiro Kurihara, Tetsuya Iizuka, Makoto Ikeda, Kunihiro Asada, *U. of Tokyo*

An Evolutionary Synthesis Algorithm to Design Optimum Performance CMOS RFSSCAs
 Luis Mendes, *Instituto Politecnico de Leiria / Instituto de Telecomunicações*; Eduardo Pires, *U. de Trás-os-Montes e Alto Douro*; João Vaz, Maria Rosário, *Instituto Superior Técnico / Instituto de Telecomunicações*

C5L-A Current Mode Circuits

Place: Auditorium

Chair: Said Belkouch; *ENSA Marrakech, Morocco*

Design and Verification of Ultra Low Current Mode Amplifier Aiming at Biosensor Applications

Lei Zhang, Zhiping Yu, Xiangqing He, *Tsinghua U.*

High Speed, Low Power Four-Quadrant CMOS Current-Mode Multiplier

Ali Naderi, Abdollah Khoei, Khayrollah Hadidi, *Urmia U.*

Transformation from Voltage-Mode to Current-Mode: an Alternative Approach

Özhan Koca, *U. of Erlangen-Nuremberg*; Xinyi Yang, *Tongji U., Shanghai, China*; Robert Weigel, *U. of Erlangen-Nuremberg*

A Low-Voltage Integrated Current-Mode Boost Converter for Portable Power Supply

Hou-Ming Chen, Robert C. Chang, Jian-Lin Wu, *National Chung-Hsing U.*

A CMOS Current-Mode Hyperbolic-Sine-Based Three-Electrode Sensor Interfacing and Amplification Circuit

Anoop Singh Walia, Henry Man Ip, Andreas Katsiamis, Emmanuel Drakakis, *Imperial College London*

C5L-B Low-Noise CMOS Design

Place: Room 1

Chair: Ahmed El Oualkadi; *ENSA Marrakech, Morocco*

Low Noise and Low Cost Neural Amplifiers

Guilherme Bontorin, Jean Tomas, Sylvie Renaud, *U. of Bordeaux 1*

A Low Power V-Band Low Noise Amplifier Using 0.13- μm CMOS Technology

Chung-Yu Wu, *National Chiao Tung U.*; Po-Hung Chen, *National Chiao-Tung U.*

System-Design-Oriented Low Noise Amplifier Modeling

Benjamin Nicolle, *Mentor Graphics - Laboratoire d'Electronique Antennes & Télécommunications*; Mourad Zaarour, William Tatinian, Gilles Jacquemod, *Laboratoire d'Electronique Antennes & Télécommunications*

A Low Noise CMOS Preamplifier for Quartz-Based Gyro-Meter

Ming Zhang, Nicolas Llaser, *U. of Paris XI*

A Novel LNA Topology with Transformer-Based Input Integrated Matching and its 60-GHz Millimeter-Wave CMOS 65-nm Design

Domenico Zito, Domenico Pepe, Bruno Neri, *U. of Pisa*; Thierry Taris, Jean-Baptiste Begueret, Yann Deval, *U. of Bordeaux*; Didier Belot, *STMicroelectronics*

C5L-C Wireless System Design

Place: Room 2

Chair: Ahmed Tewfik; *U. of Minnesota, USA*
Mustapha Alami, *INPT, Morocco*

Theoretical and Practical Limits to Sensitivity in IEEE 802.15.4 Receivers
Steven Lanzisera, Kristofer Pister, *U. of California, Berkeley*

Sustainability of Self-Configuring Wireless Sensor Networks
Bozena Kaminska, *Simon Fraser U.*; Pawel Gburzynski, *U. of Alberta*

Ultra Low Power ASIP Design for Wireless Sensor Nodes
Michael De Nil, *IMEC-NL and Eindhoven U. of Technology*; Lennart Yseboodt, *Philips Research / Eindhoven U. of Technology*; Frank Bouwens, Jos Hulzink, *IMEC-NL*; Mladen Berekovic, *IMEC-NL and Technical U. Delft*; Jos Huisken, *Silicon Hive*; Jef van Meerbergen, *Philips Research / Eindhoven U. of Technology*

Vertical Handover for 4G Multi-Standard Wireless Transceivers
Zongyang Zhao, Jad G. Atallah, Ana Rusu, Mohammed Ismail, *Royal Institute of Technology*

Fast Secure Communication Establishing Mechanism for Aero-Wireless Networks
Kihong Kim, *Korea U.*; Jinkeun Hong, *Baekseok U.*; Jongin Lim, *Korea U.*

C5L-D Statistical Signal Processing

Place: Room 3

Chair: M. Omair Ahmad; *Concordia Univ, Montreal, USA*
Ahmed Bouridane; *Queens U., Belfast, UK*

Iterative Noise-Compensated Method to Improve LPC Based Speech Analysis
Abdelaziz Trabelsi, *École Polytechnique de Montréal*; Mounir Boukadoum, *U. du Québec à Montréal*; François Raymond Boyer, Yvon Savaria, *École Polytechnique de Montréal*

Adaptive Selectivity Representation: Construction and Application in Enhancement
Mohamed El Aallaoui, Abdelmoula El Bouhtouri, *Faculté des Sciences ElJadida-Morocco*; Abderahman Ayadi, *Ecole Nationale des Sciences Appliquées*

On the Performance of Non-Gaussian Distributions in Modelling the Wavelet Coefficients of Medical Ultrasound Images
M.I.H. Bhuiyan, M. Omair Ahmad, M.N.S. Swamy, *Concordia U.*

Referenced Contrast: a New Tool for Blind Separation of Gaussian Sources
Manal Taoufiki, *LRIT GSCM*; Abdellah Adib, *Institut Scientifique, Rabat*; Driss Aboutajdine, *LRIT-GSCM, U. Mohamed V Rabat*

Estimation of Displacement Vector Field from Noisy Data Using Maximum Likelihood Estimator
Ismaili Alaoui El Mehdi, *U. Mohamed V Rabat Agdal Morocco*; Ibn El Haj Elhassane, *National Institute of Post and Telecommunications, Rabat-Morocco*

C5L-E Frequency Synthesizers, Filters and Mixers

Place: Room 4

Chair: Fernando Azevedo; *Instituto Superior de Engenharia de Lisboa, Portugal*
Wenceslas Rahajandraibe; *U. of Provence, France*

A Fast-Locking Agile Frequency Synthesizer for MIMO Dual-Mode WiFi / WiMAX Applications

Meng-Ting Tsai, *Industrial Technology Research Institute/SoC Technology Center*; Ching-Yuan Yang, *National Chung-Hsing U.*

A Low-Noise Fractional-N Frequency Synthesiser Using a Very Fast Noise Shaper

Hongyu Wang, Paul Brennan, Dai Jiang, *U. College London*

A Fractional Frequency Synthesizer Using Frequency Locked Loop

Rejeesh A. V., Pradip Mandal, *Indian Institute of Technology Kharagpur*

Discrete-Time Decimation Filter Design for Multistandard RF Sub-Sampling Receiver

Rim Barrak, *Ecole Supérieure des Communications*; Adel Ghazel, *Ecole Supérieure des Communications de Tunis*; Fadel Ghannouchi, *U. of Calgary*

A 1.4GHz Upconversion Mixer Design Using the gm/ID Method Suitable for a Multi-Band Analog Interface

Fernando Paixao Cortes, *U. Federal do Rio Grande do Sul*; Sergio Bampi, *Federal U. of Rio Grande do Sul*

C5L-F Power Considerations at the Architecture Level

Place: Room 5

Chair: Ahmed Nabil Belbachir; *Austrian Research Centers, Austria*
Denizar Cruz Martins; *Federal U. of Santa Catarina, Brazil*

Building Ultra-Low-Power Low-Frequency Digital Circuits with High-Speed Devices

David Bol, Renaud Ambroise, Denis Flandre, Jean-Didier Legat, *U. Catholique de Louvain*

Power Analysis Resistant Hardware Implementations of AES

Levent Ordu, *TUBITAK*; Berna Ors, *Istanbul Technical U.*

A Low-Power Integrated Neural Interface with Digital Spike Detection and Isolation

Benoit Gosselin, Mohamad Sawan, *École Polytechnique de Montréal*

LUT-Based Power Macromodeling Technique for DSP Architectures

Yaseer A. Durrani, Teresa Riesgo, *Universidad Politécnica de Madrid*

Friday, December 14, 2007, 15:35 - 16:00

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