



DIRO
IFT 1215

DÉMONSTRATION N° 3

Max Mignotte

DIRO, Département d'Informatique et de Recherche Opérationnelle, local 2377.

[http : //www.iro.umontreal.ca/~mignotte/ift1215/](http://www.iro.umontreal.ca/~mignotte/ift1215/)

E-mail : mignotte@iro.umontreal.ca

Exercices tirés du livre de V.P. Heuring and H.F. Jordan
Computer Systems Design and Architecture, 1997.

Photocopies distribuées en classe de démonstration

Annexe 1	Circuits Combinatoires
Exercices numéro	A.1-A.10 (Portes logiques, Algèbre de Boole, Synthèse) A.12, A.15 (Multiplexeurs, Decodeurs) A.27, A.28 (Simplification, Tableau de Karnaugh)

A.1

1. Show the logic diagram for an OR gate implemented with a NAND gate and inverters.
2. Show the logic diagram of an inverter implemented with NAND gates.
3. Show the logic diagram for an AND gate implemented entirely with NAND gates.

A.2

Draw logic diagrams for each member of the computationally complete set [AND, OR, NOT], using only the computationally complete set [NOR].

A.3

Given the following logic circuit, construct a truth table that describes its behavior.

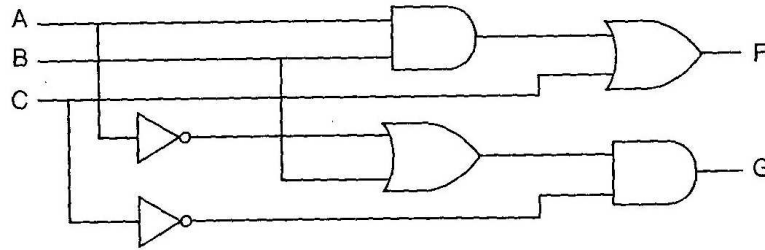


FIGURE 1 – A logic circuit

A.4

Construct a truth table for a three-input XOR gate.

A.5

Compute the gate input count of the 4-to-2 priority encoder shown in Figure 2. Include the inverters in your count.

A.6

Design a circuit that implements function f , using AND, OR, and NOT gates.

$$f(A, B, C) = \bar{A}BC + \bar{A}\bar{B}\bar{C} + AB\bar{C} \quad (1)$$

A.7

Design a circuit that implements function g , using AND, OR, and NOT gates. Do not attempt to change the form of the equation.

$$g(A, B, C, D, E) = \bar{A}(BC + \bar{B}\bar{C}) + B(CD + E) \quad (2)$$

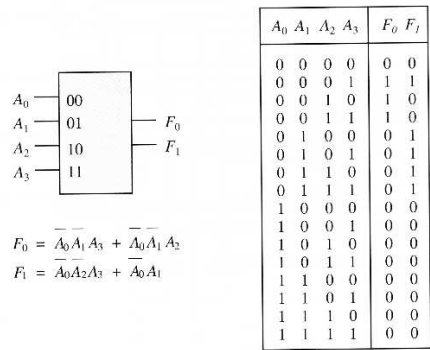


FIGURE 2 – A 4-to-2 priority encoder

A.8

Are function f and g equivalent? Show how you arrived at your answer.

$$f(A, B, C) = ABC + \overline{A}B\overline{C} \qquad g(A, B, C) = (A \oplus C)B$$

A.9

Write a Boolean equation that describes function F in the following circuit. Put your answer in SOP form (without parentheses).

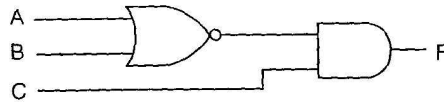


FIGURE 3 – Logic circuit implementing the function F

A.10

A four-bit *comparator* is a component that takes two four-bit words as inputs and produces a single bit of output. The output is a 0 if the words are identical, and is a 1 otherwise. Design a four-bit comparator with any of the logic gates you have seen. Hint : Think of the four-bit comparator as four one bit comparators combined in some fashion.

A.12

Use two 4-to-1 MUXes to implement the following functions :

A.15

Use a 2-to-4 decoder and an OR gate to implement the XOR of two inputs A and B.

A	B	F ₀	F ₁
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

A.27

Given the following functions, construct K-maps, and find minimal sum-of-products expressions for f and g .

$$f(A, B, C, D) = 1$$

when two or more inputs are 1; otherwise,

$$\begin{aligned} f(A, B, C, D) &= 0 \\ g(A, B, C, D) &= 1 \end{aligned}$$

when the number of inputs that are 1 is even (including the case when no inputs are 1); otherwise,

$$g(A, B, C, D) = \overline{f(A, B, C, D)}$$

A.28

Use k-maps to simplify function f and its don't care condition below. Perform the reduction for

1. the sum-of-products form
2. the product-of-sums form

$$f(A, B, C, D) = \sum(2, 8, 10, 11) + \sum_d(0, 9)$$